

FIG. 1A

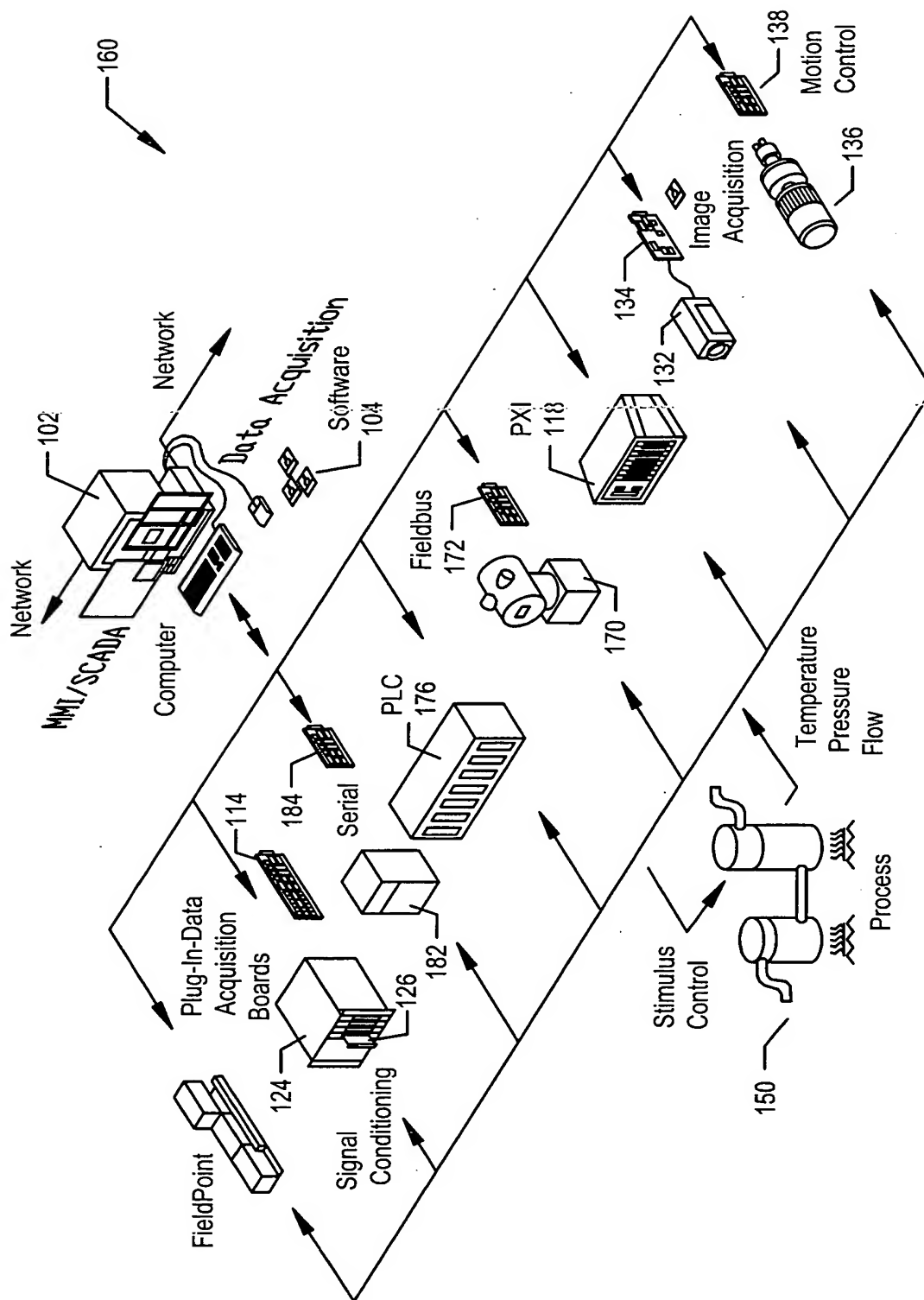


FIG. 1B

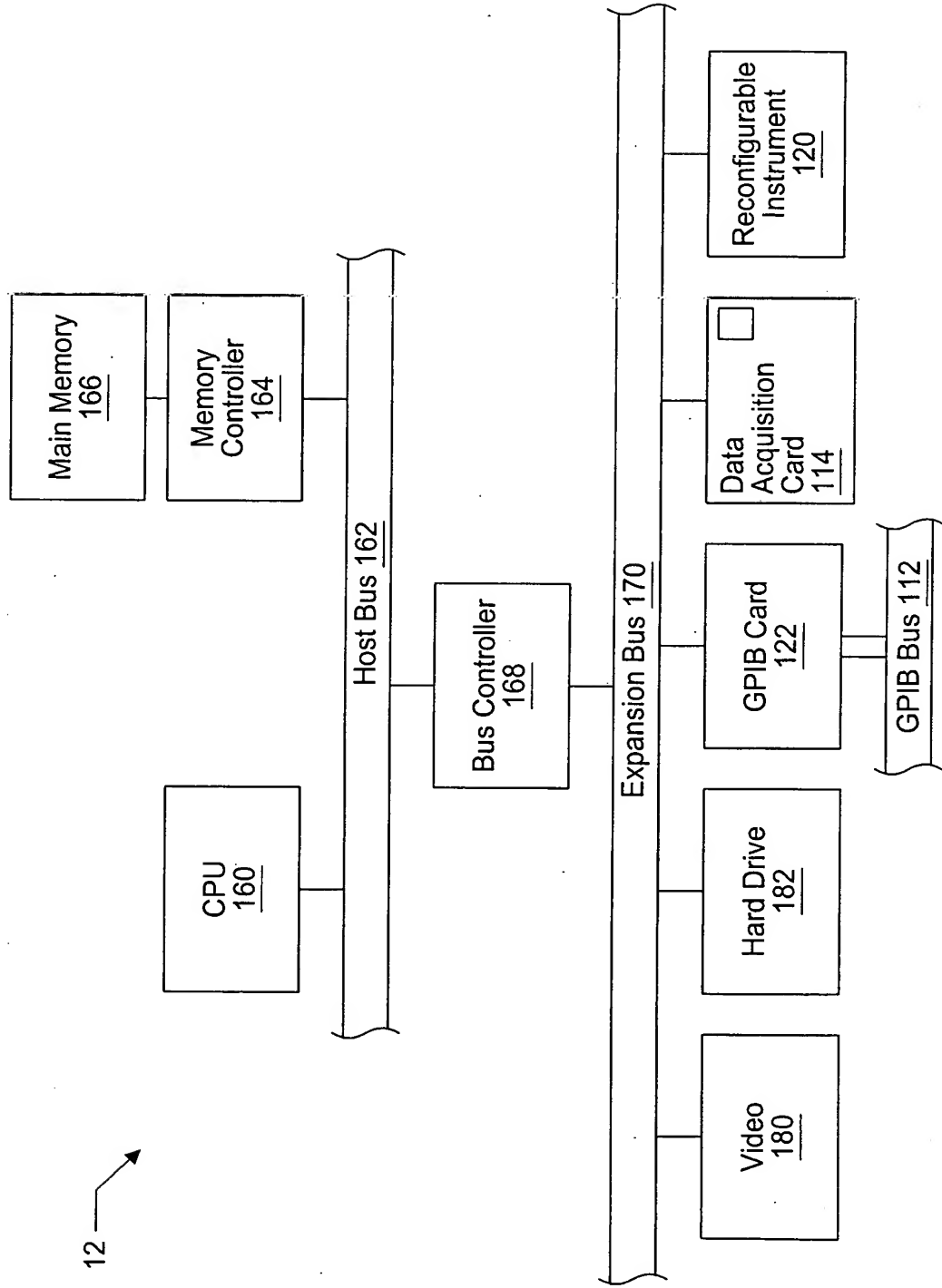


Figure 2

10003792.1 20240001

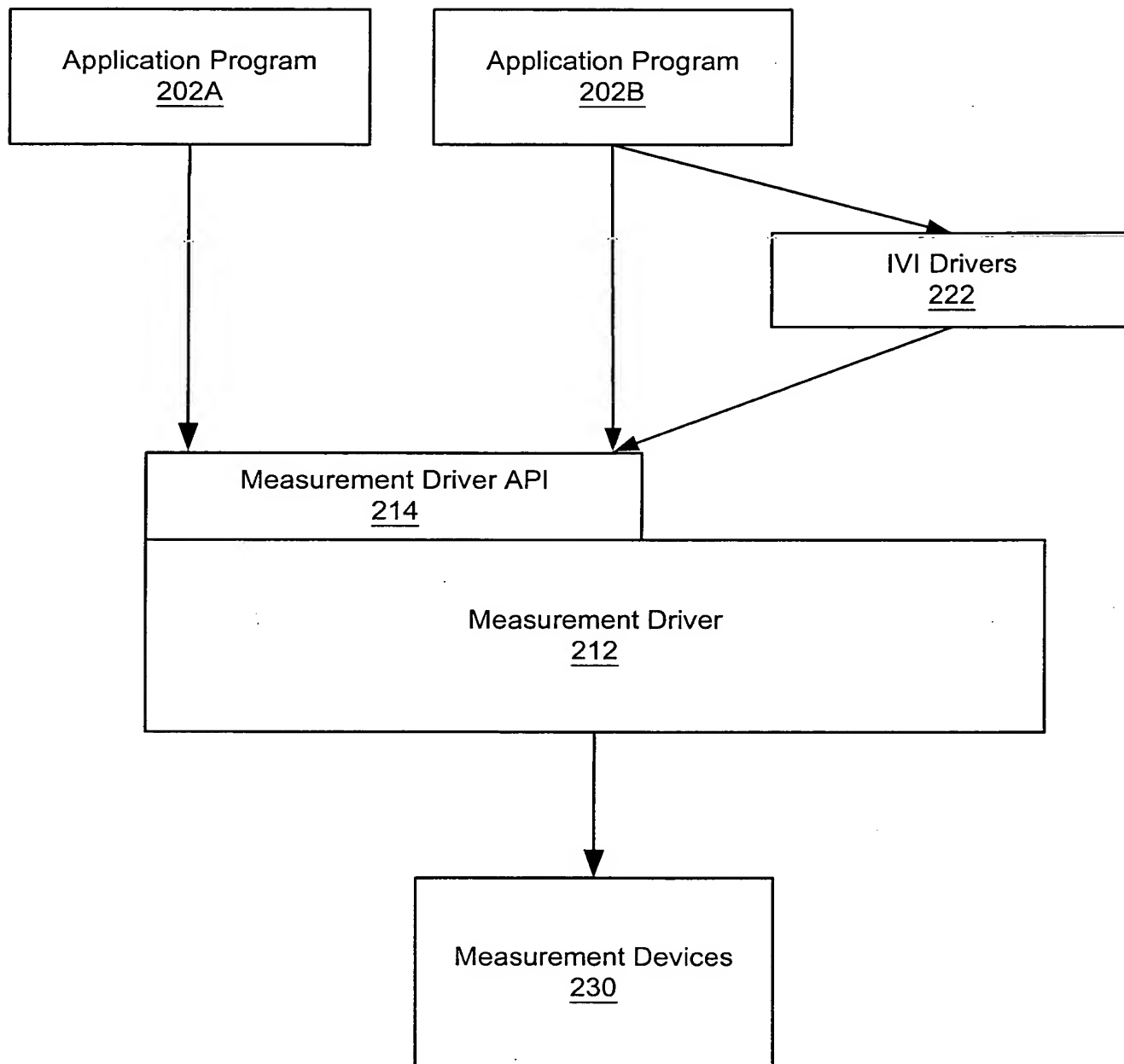


Figure 3

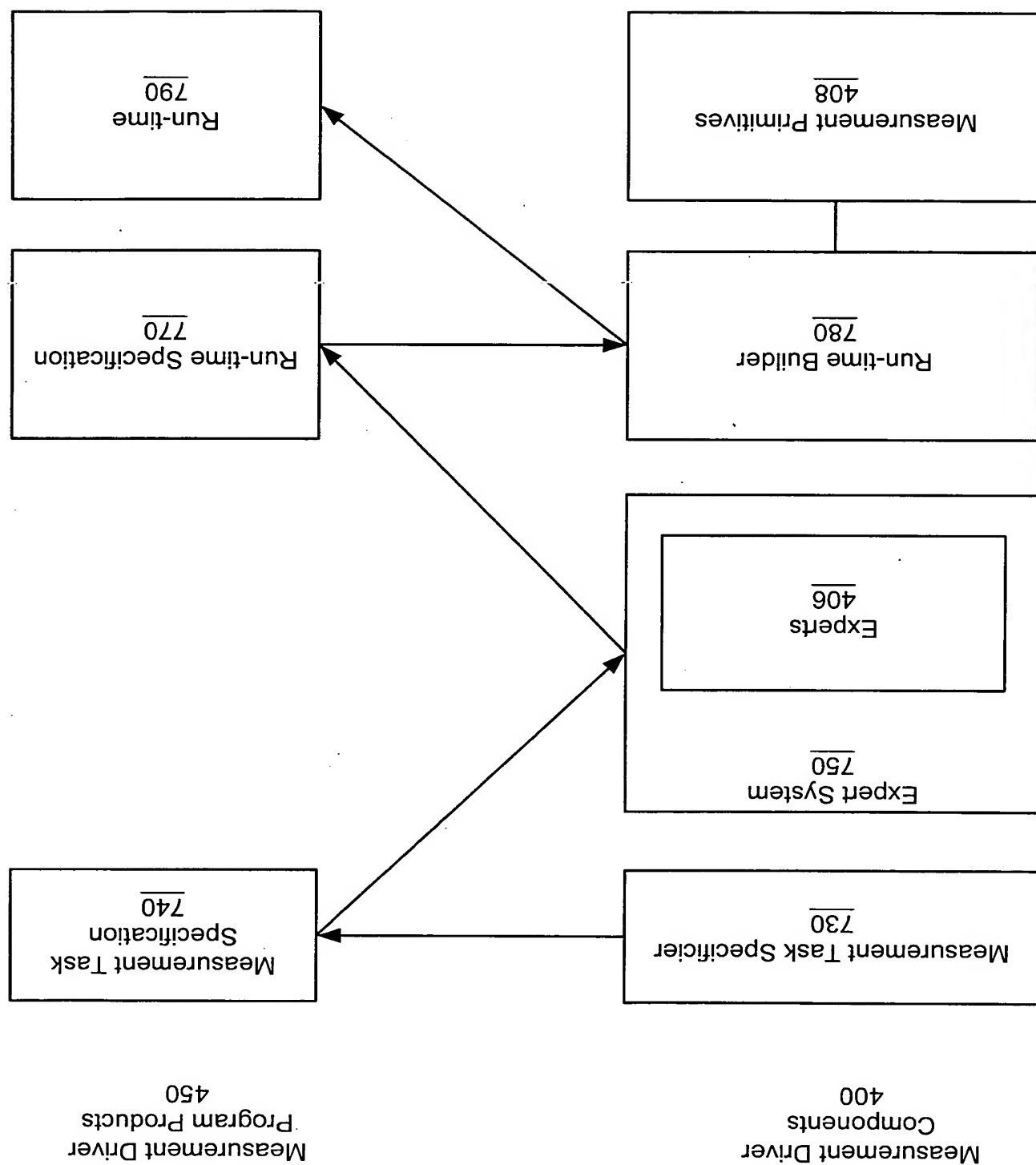


Figure 4

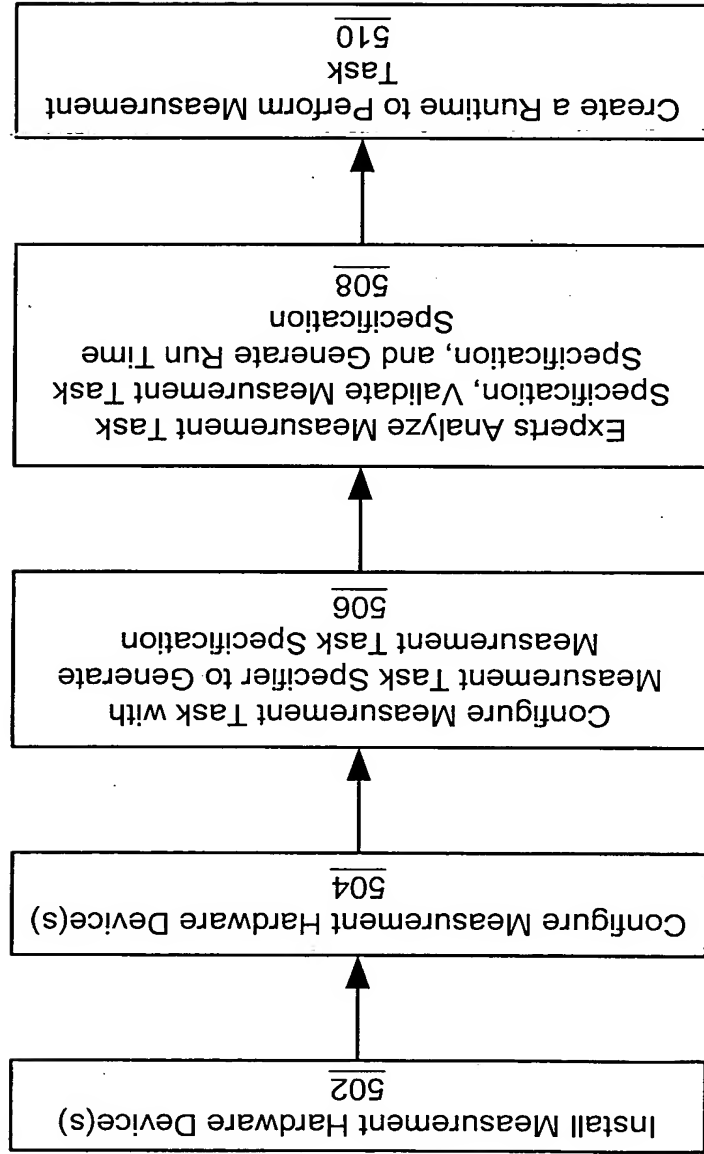
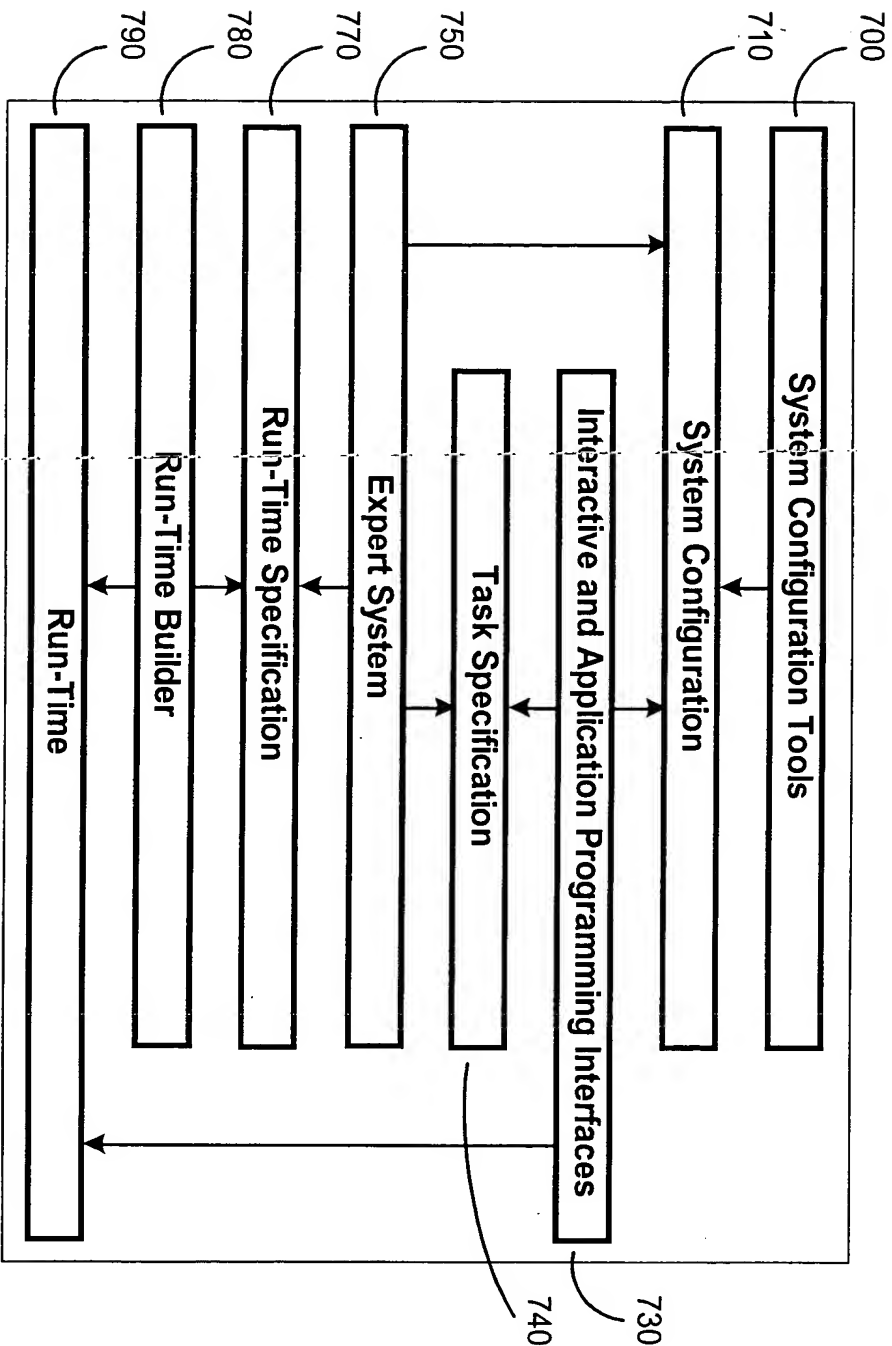


Figure 5



High-Level Architecture

Figure 6

# System Configuration and Task Specification

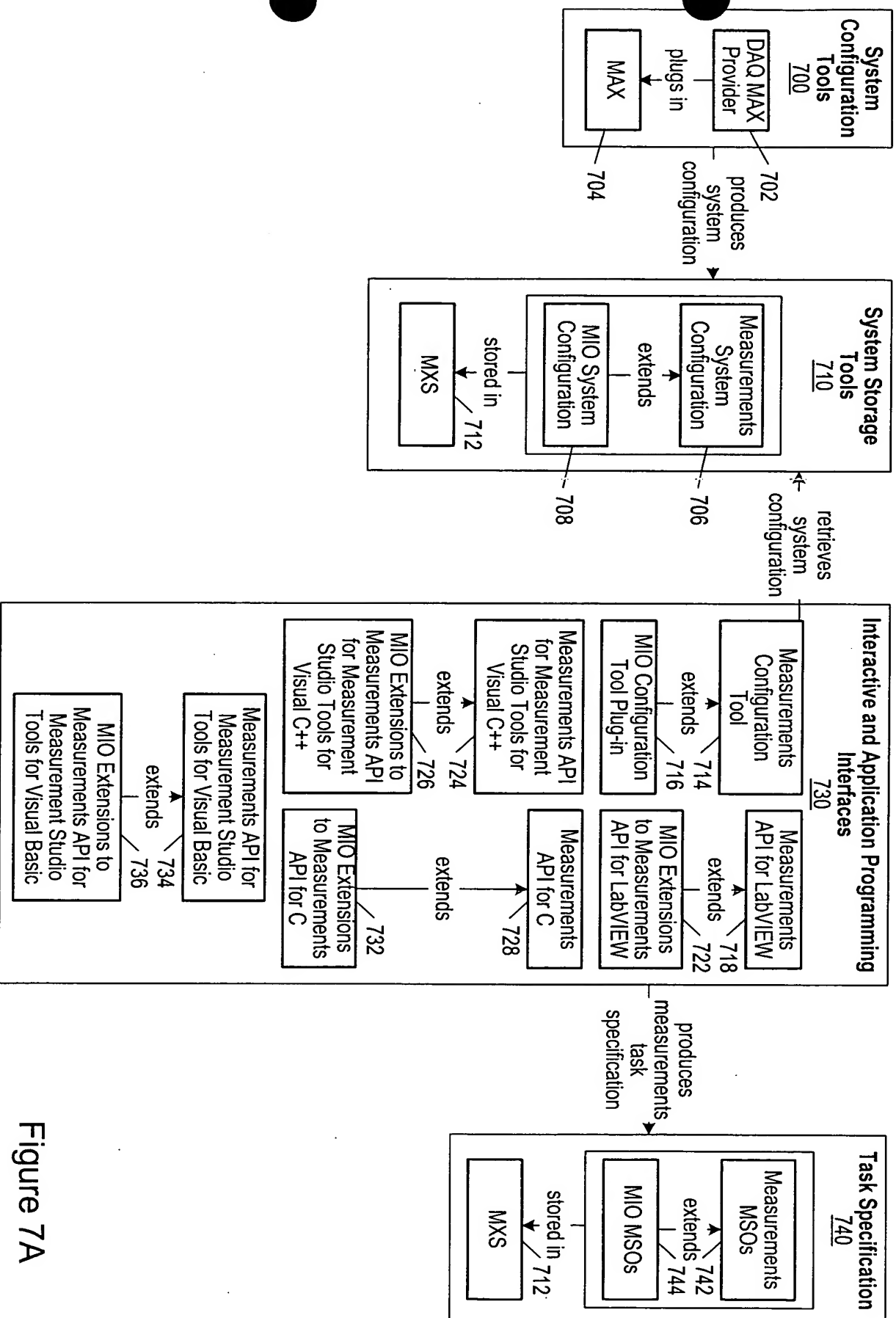


Figure 7A







## Executing Tasks

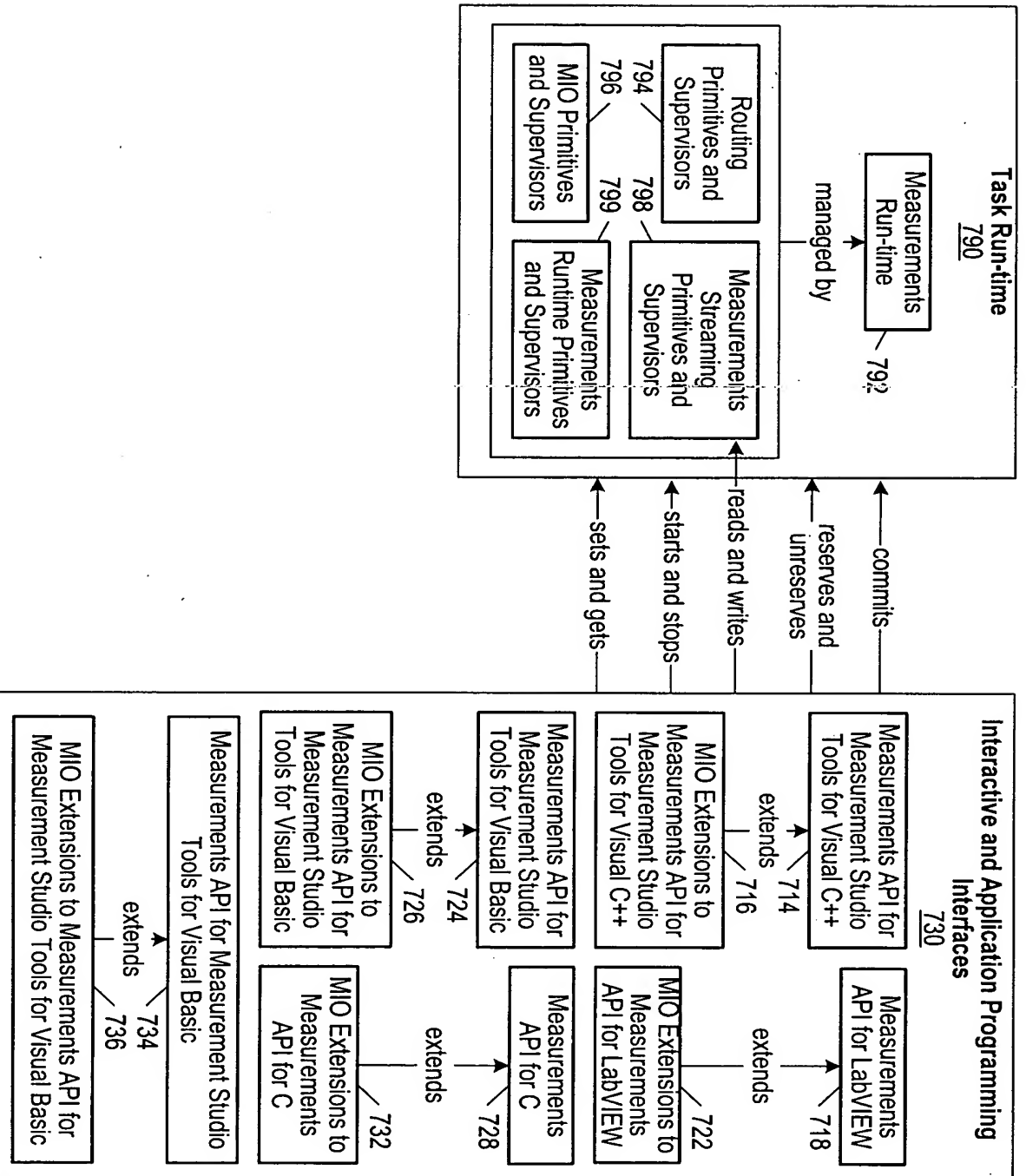


Figure 7D

# Packages for System Configuration and Task Specification

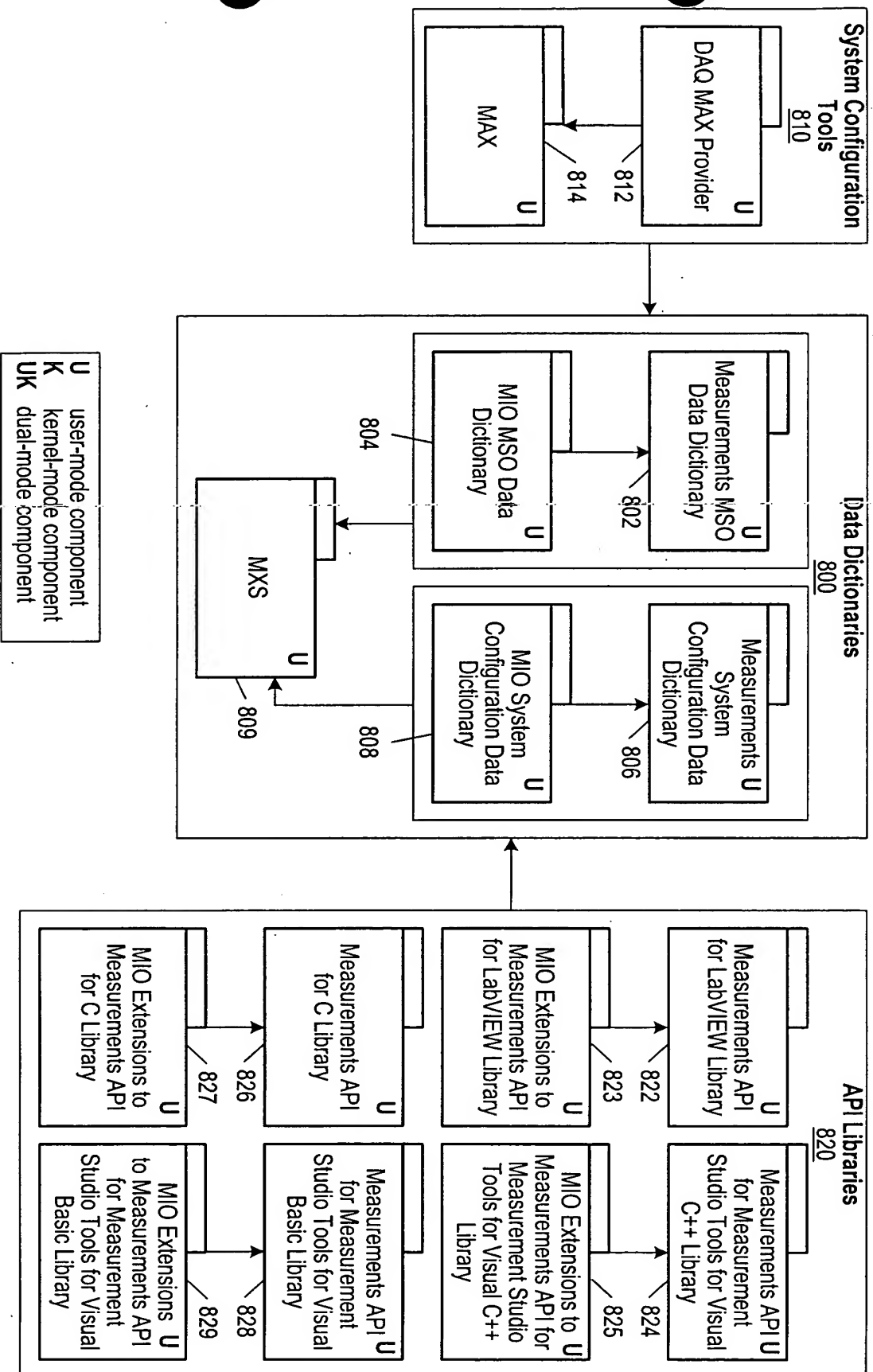


Figure 8A

# Packages for Compiling Task Specification to Run-time Specification

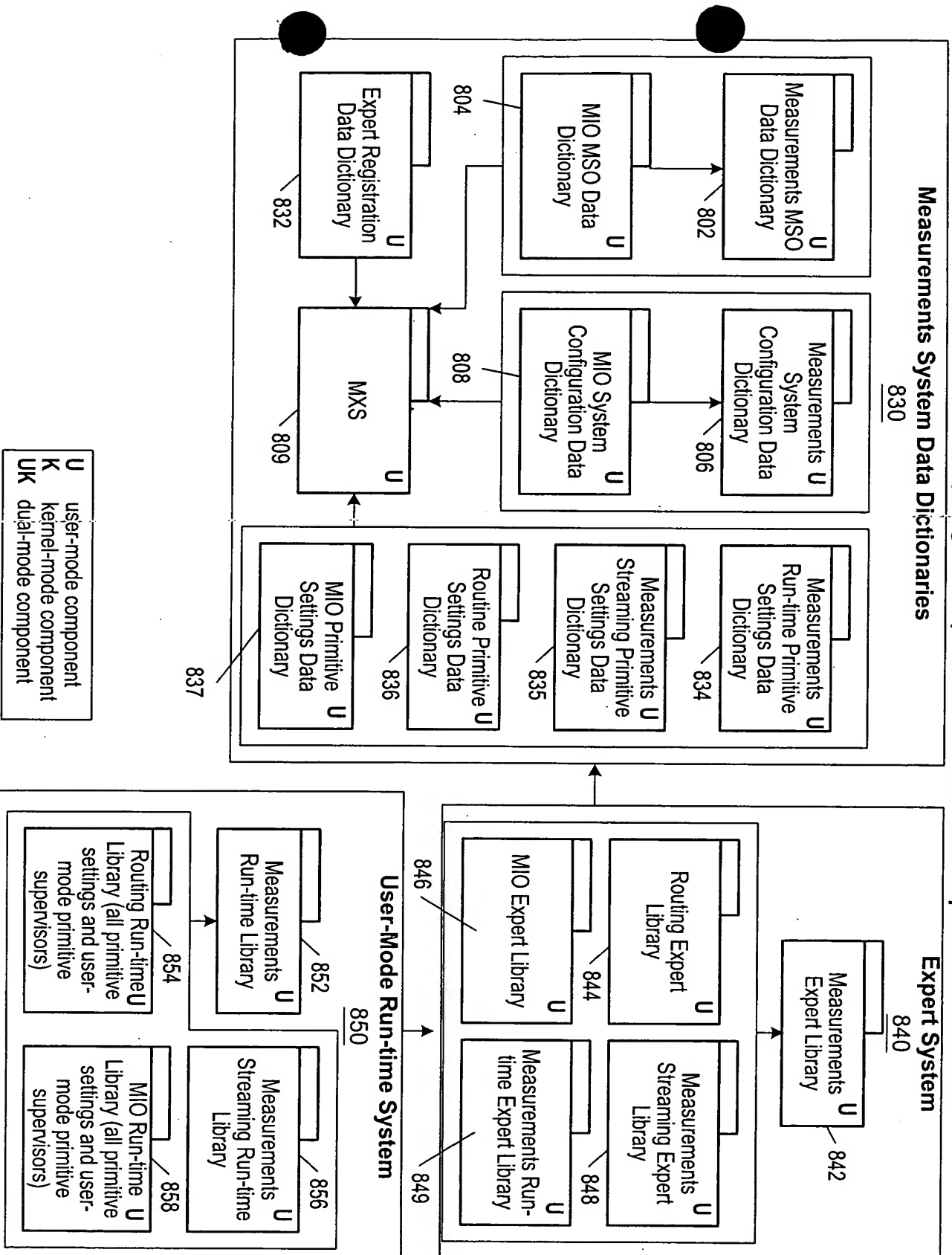


Figure 8B

# Packages for Building Task Run-time from Run-time Specification

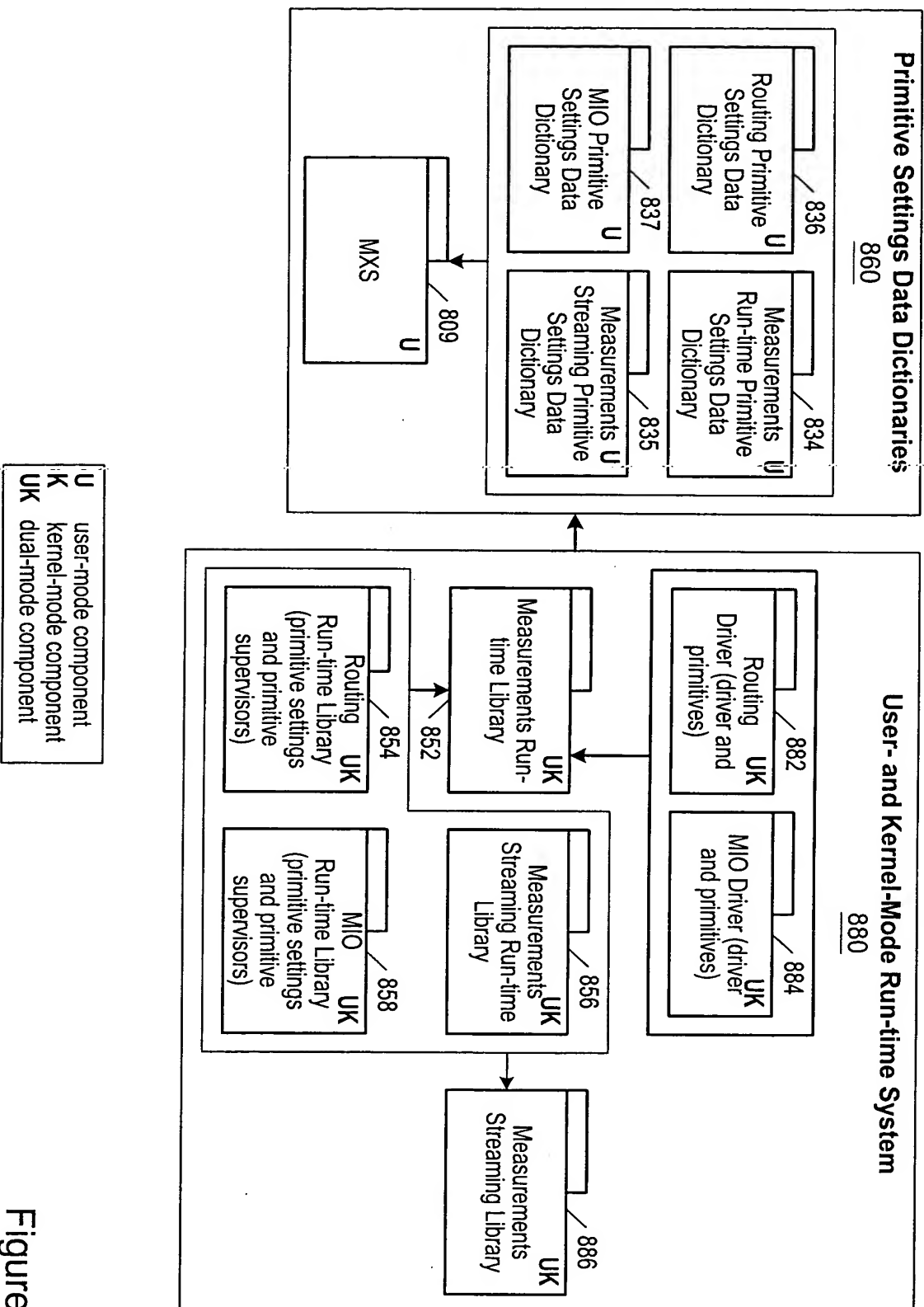


Figure 8C

# Packages for Executing Task Run-time

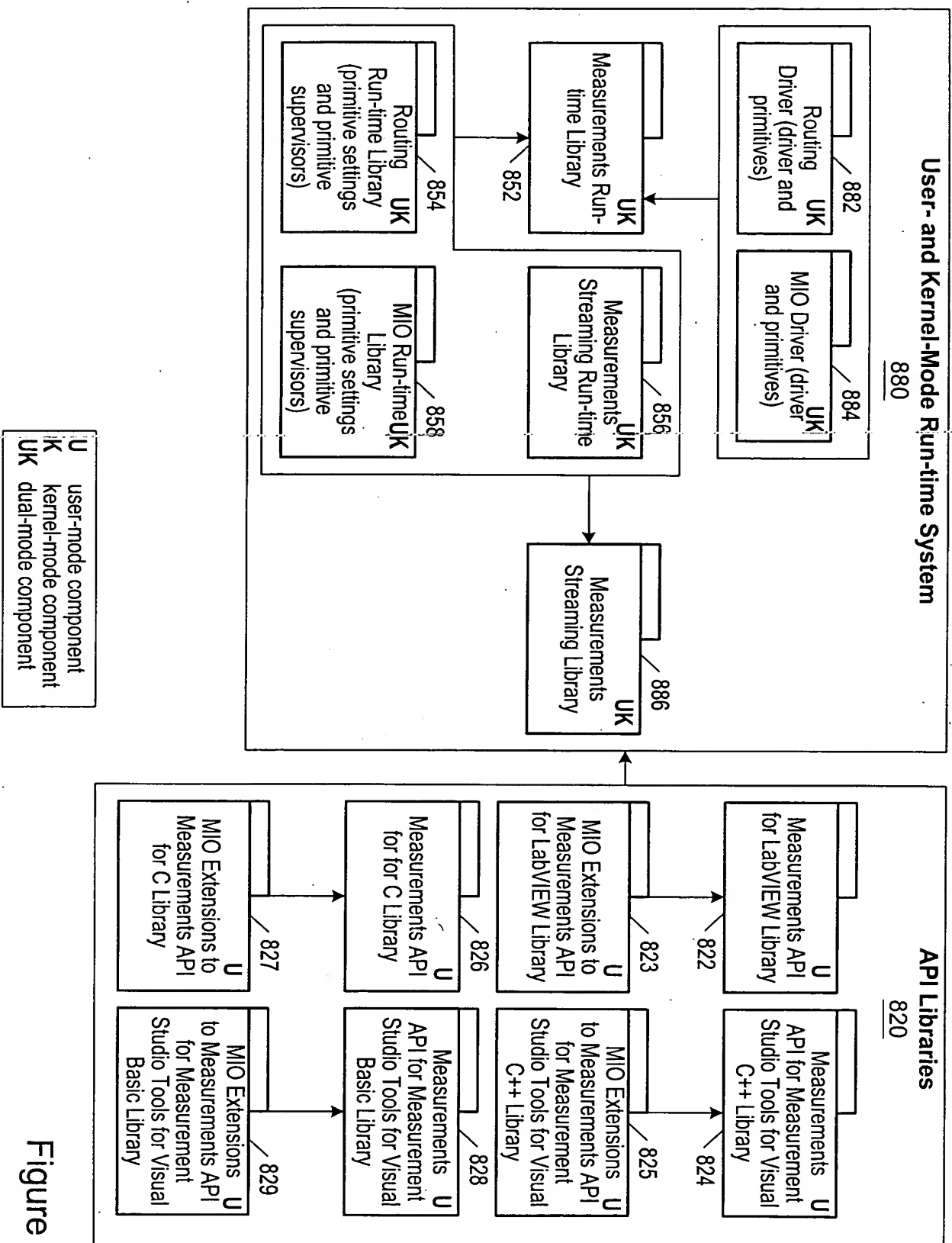


Figure 8D

## State Diagram for Measurement Tasks

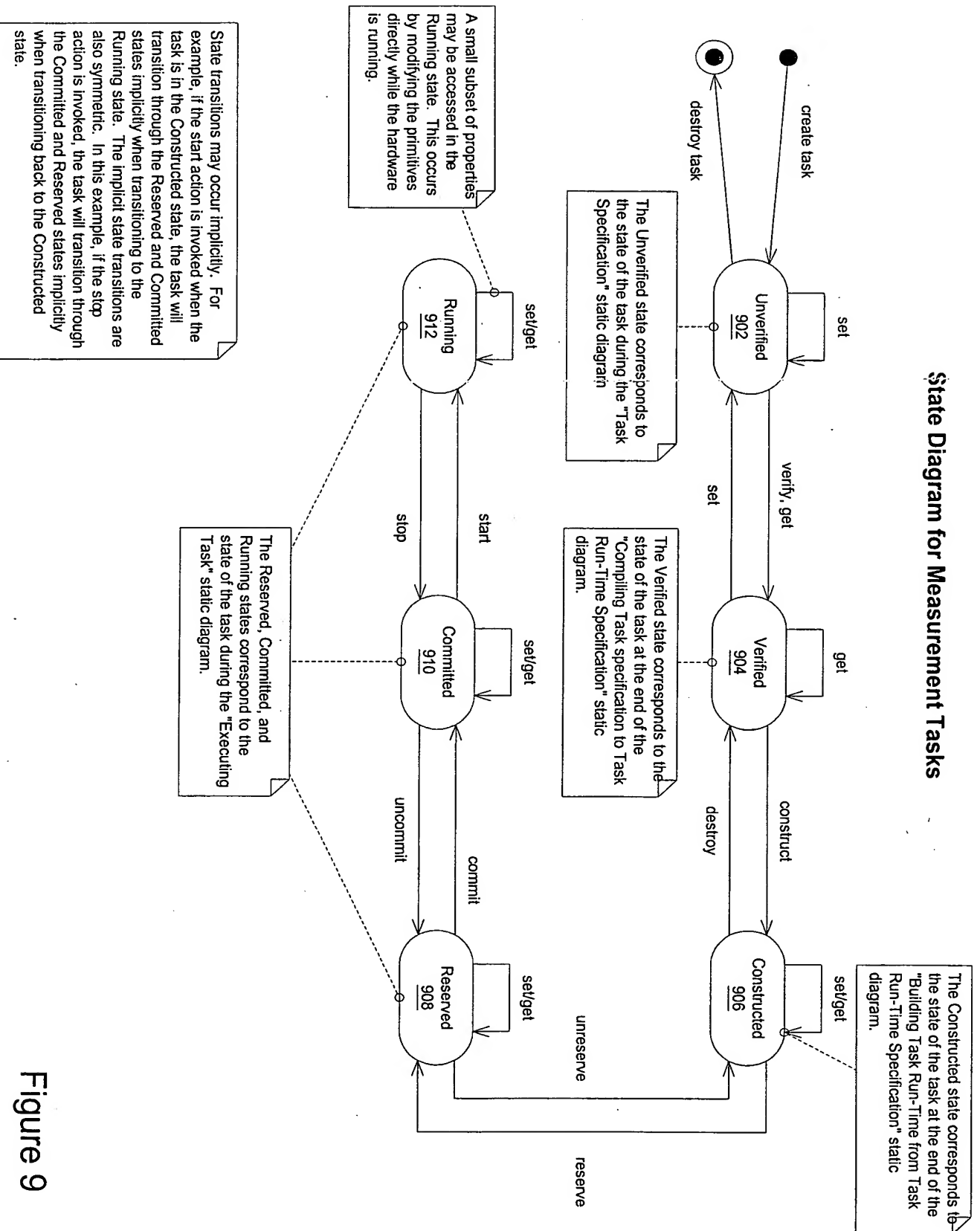


Figure 9



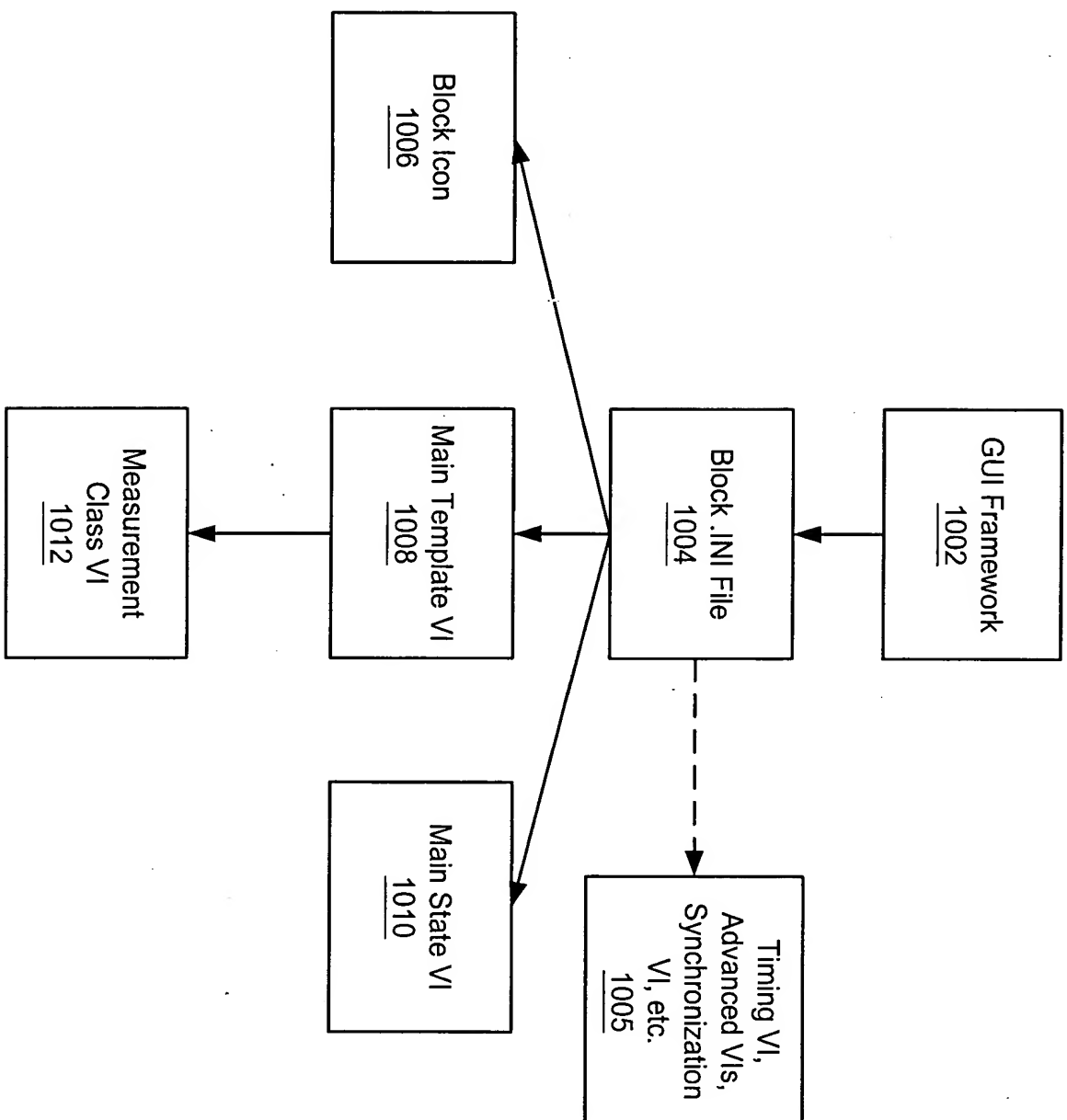


Figure 10

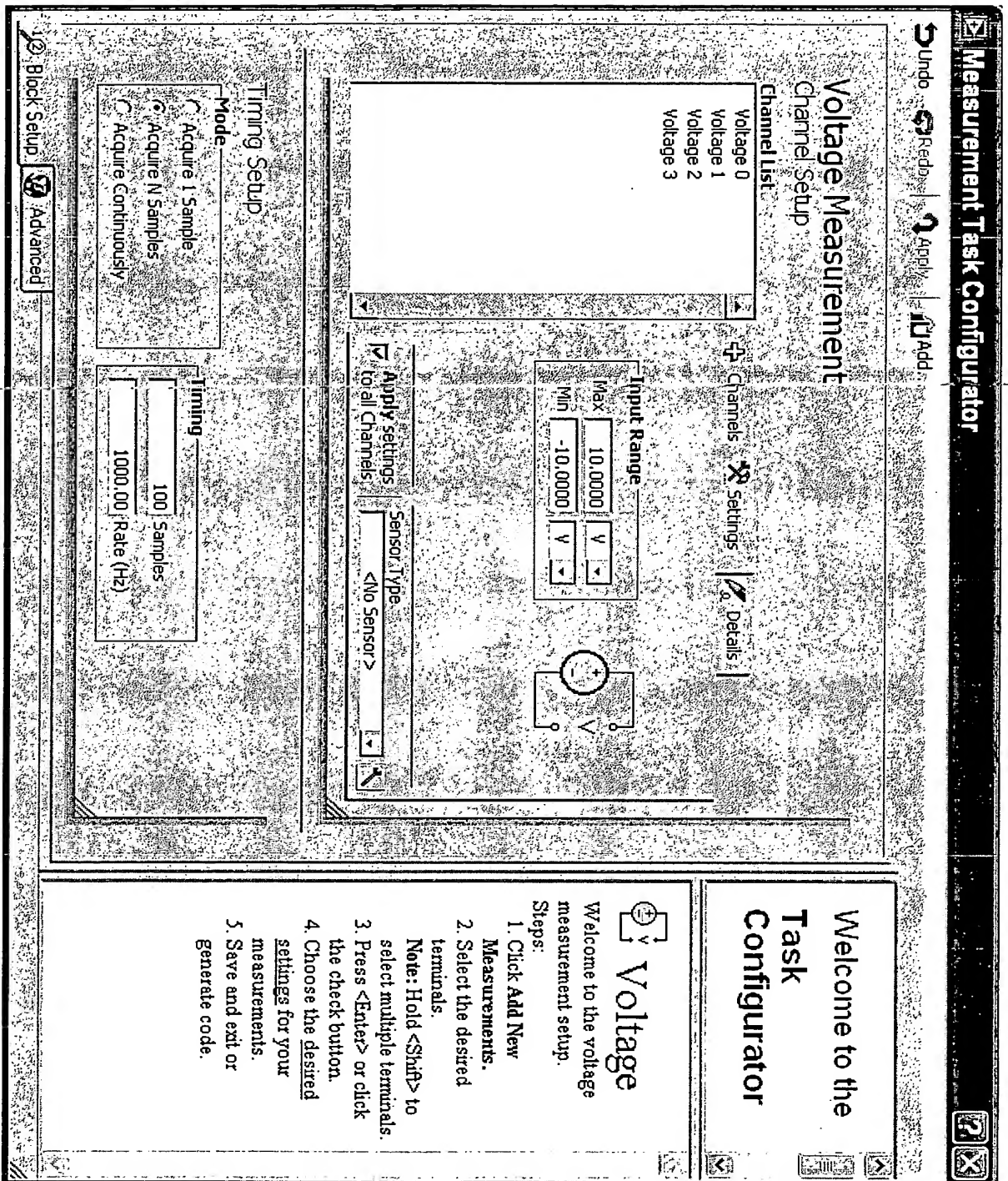


Figure 11

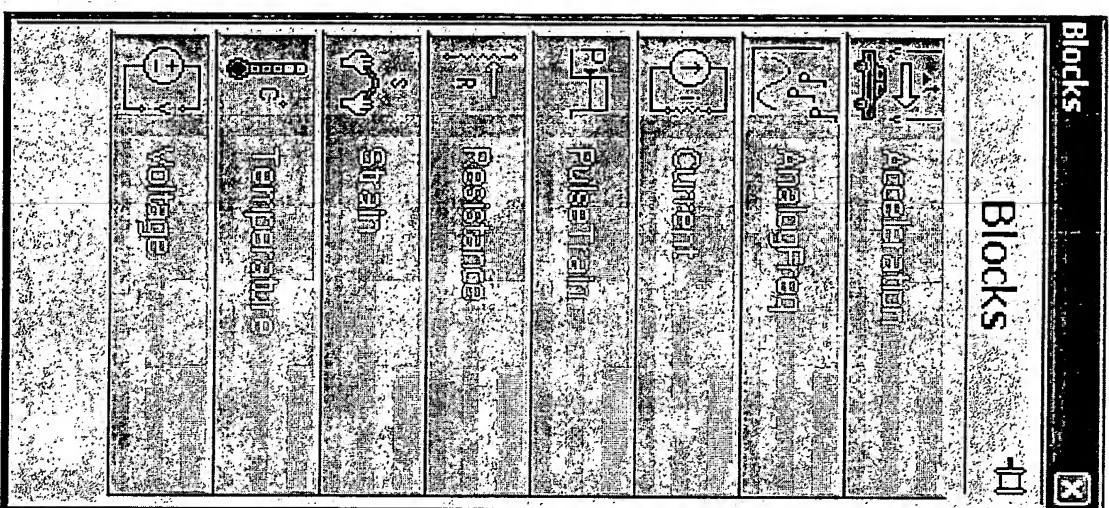


Figure 12A

Measurement Task Configurator

Undo Redo Apply Add Voltage

### Voltage Measurement

Channel Setup

Channel List

Channels

Settings

Details

Input Range

Max 10.0000 V

Min -10.0000 V

Sensor Type

<No Sensor>

Timing Setup

Mode

Acquire 1 Sample

Acquire N Samples

Acquire Continuously

Timing

100 Samples

1000.00 Rate (Hz)

Block Setup

Advanced

Welcome to the Task Configurator

Voltage

Welcome to the voltage measurement setup.

Steps:

1. Click Add New Measurements.

2. Select the desired terminals.

Note: Hold <Shift> to select multiple terminals.

3. Press <Enter> or click the check button.

4. Choose the desired settings for your measurements.

5. Save and exit or generate code.

Figure 12B

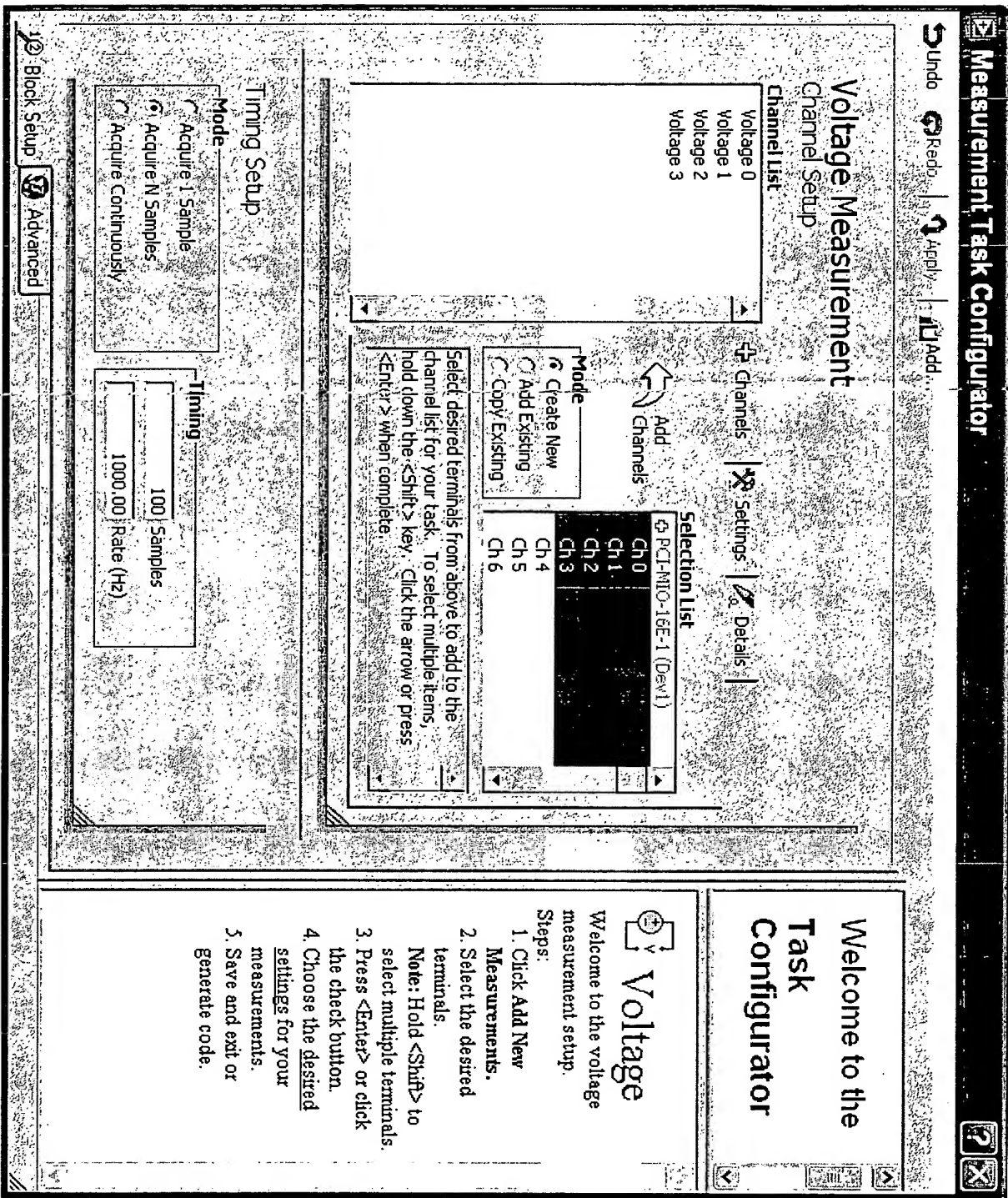


Figure 12C





## Figure 13

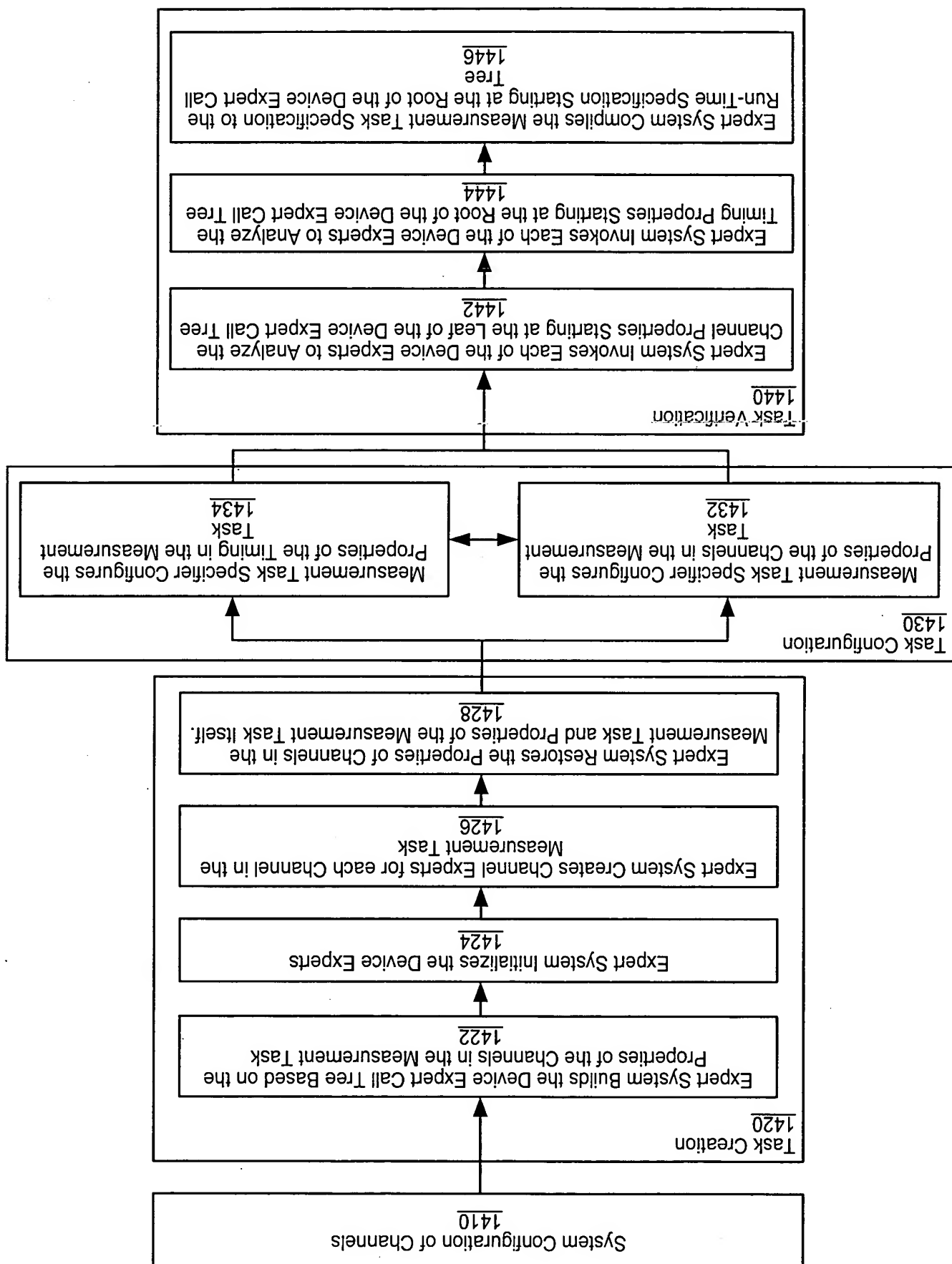


Figure 14



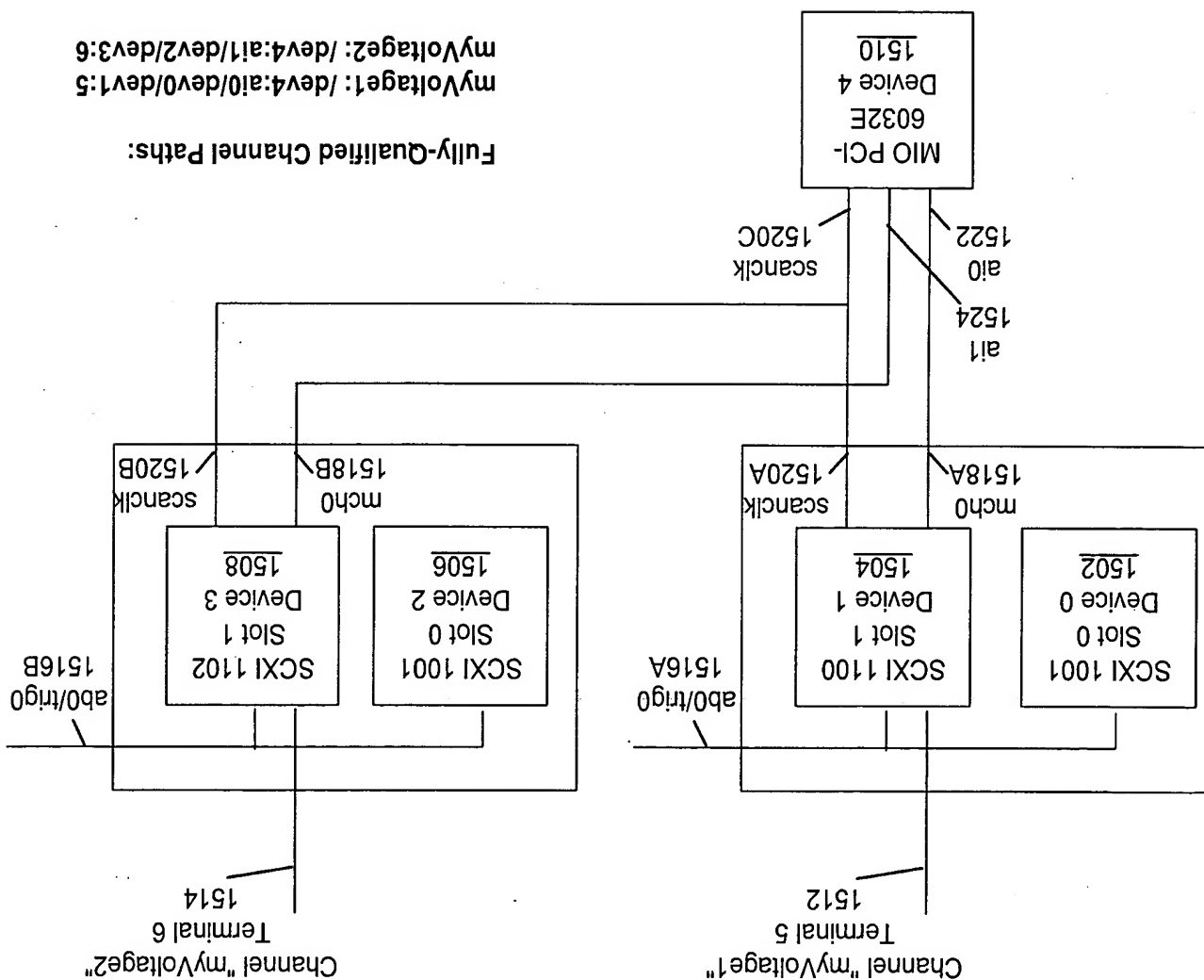
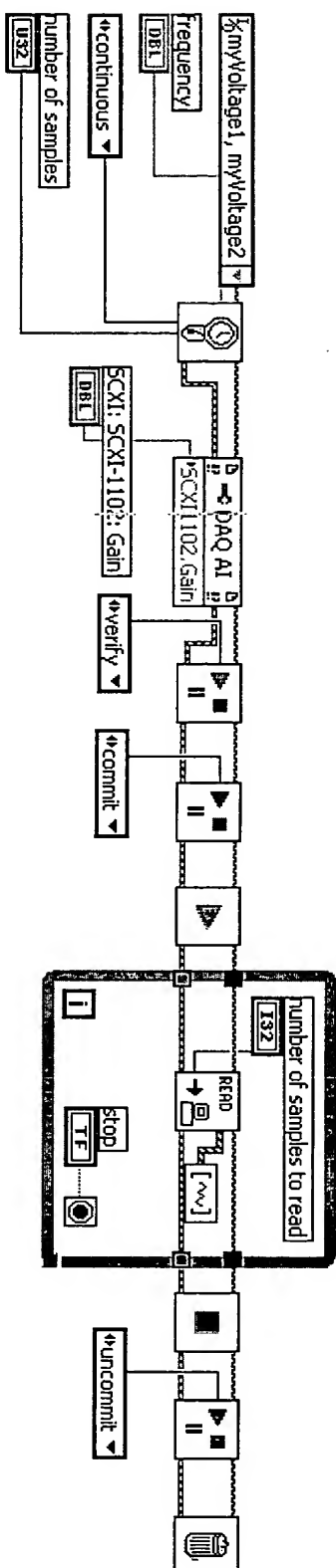


Figure 15



Voltage On Two Channels with Two SCXI Modules in Two  
SCXI Chassis Connected to an MIO DAQ Device

Figure 16

Create Device Expert Call Tree

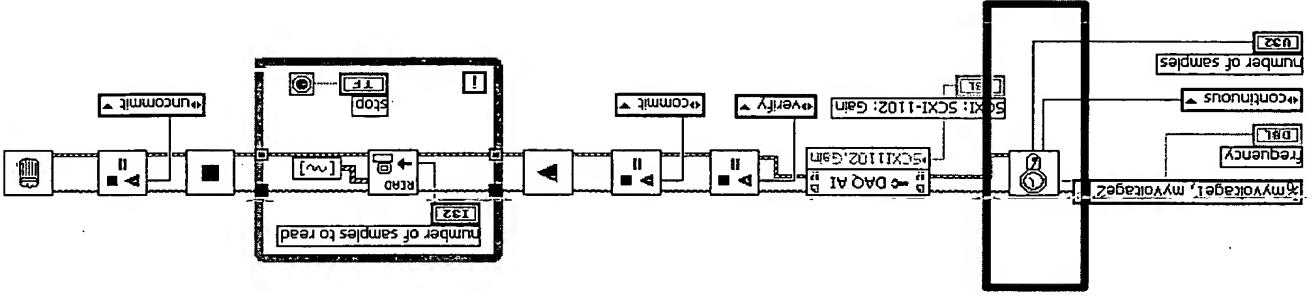
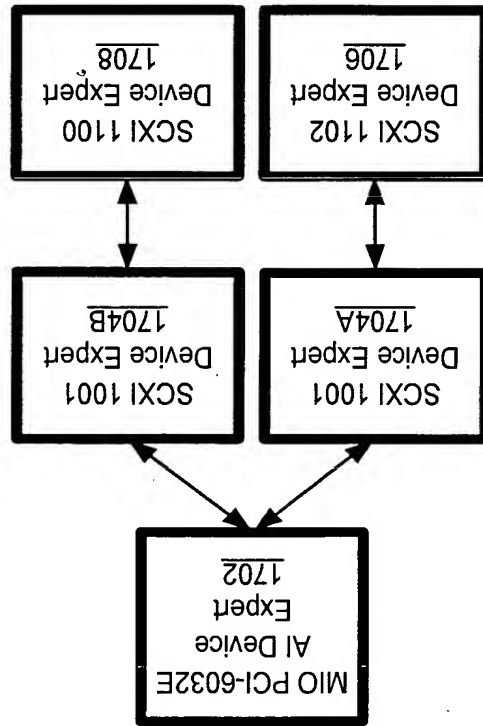
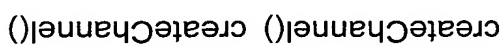
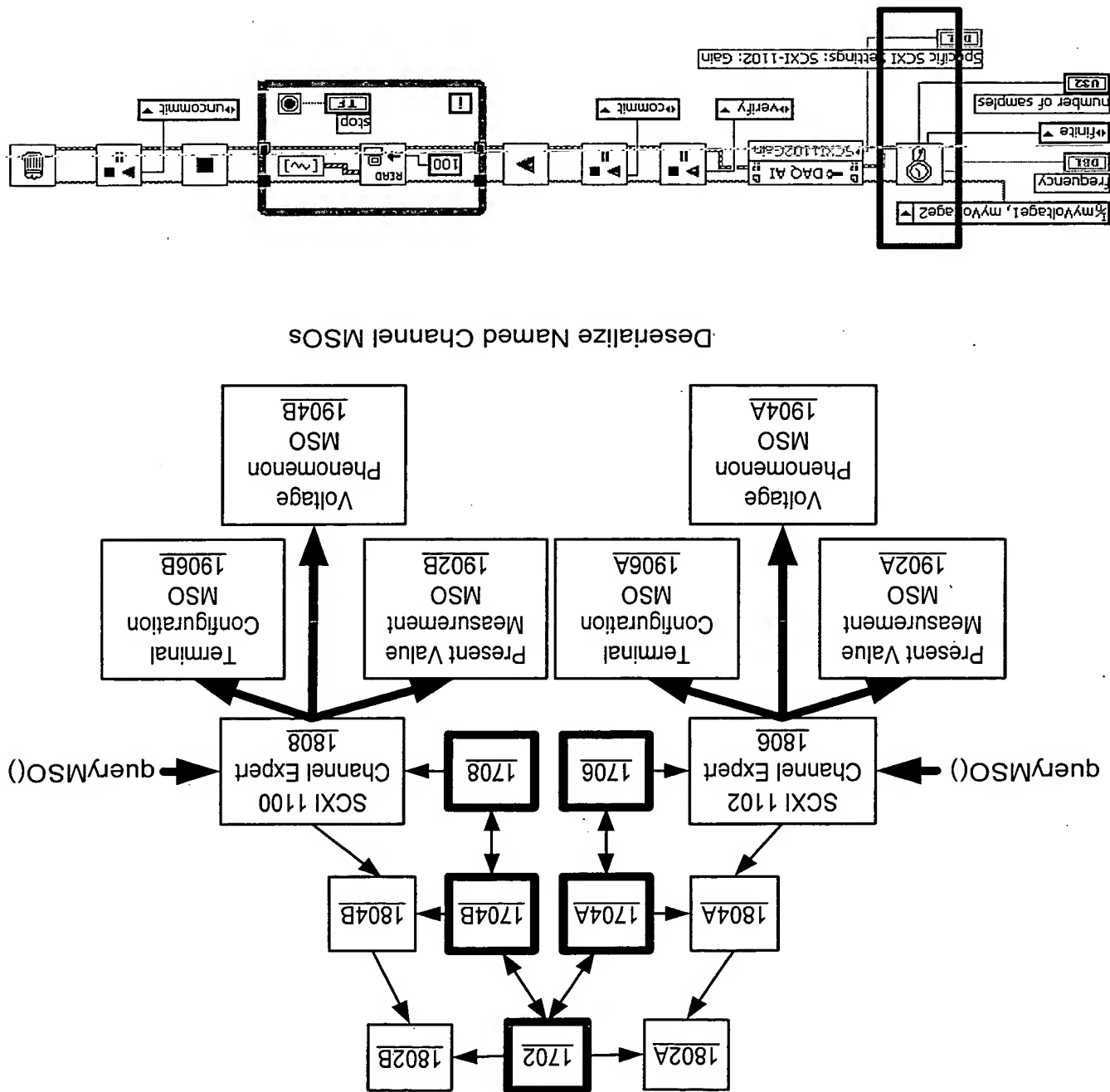


Figure 17



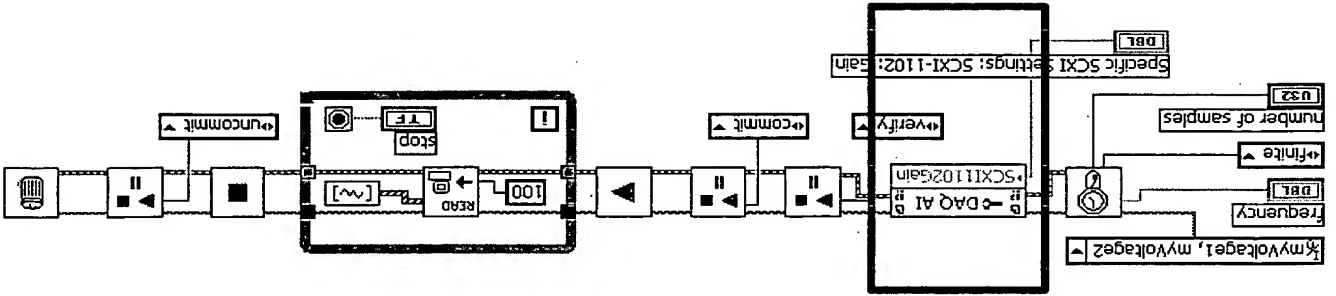
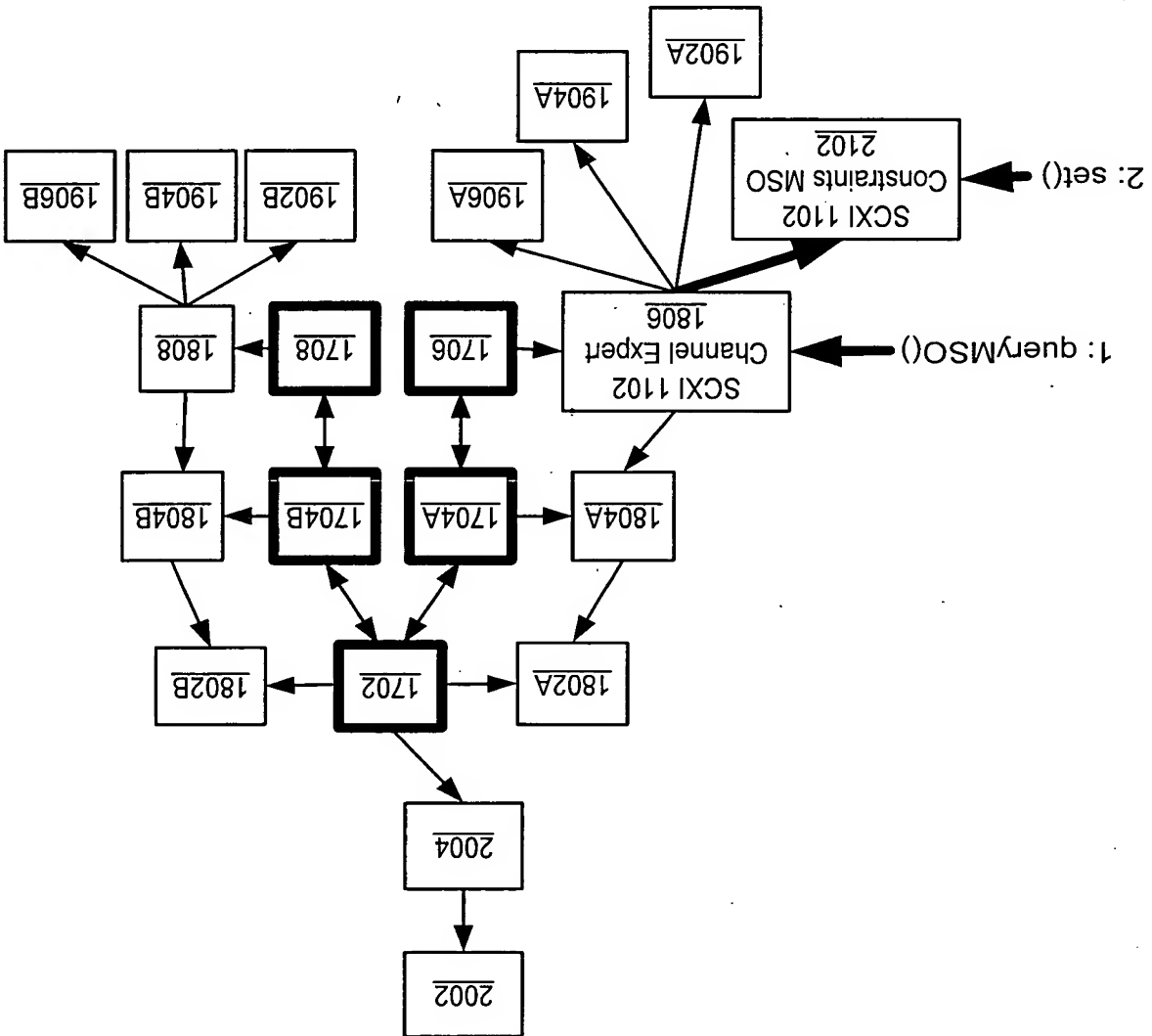
## Create Channel Experts





## Configure Timing Experts.





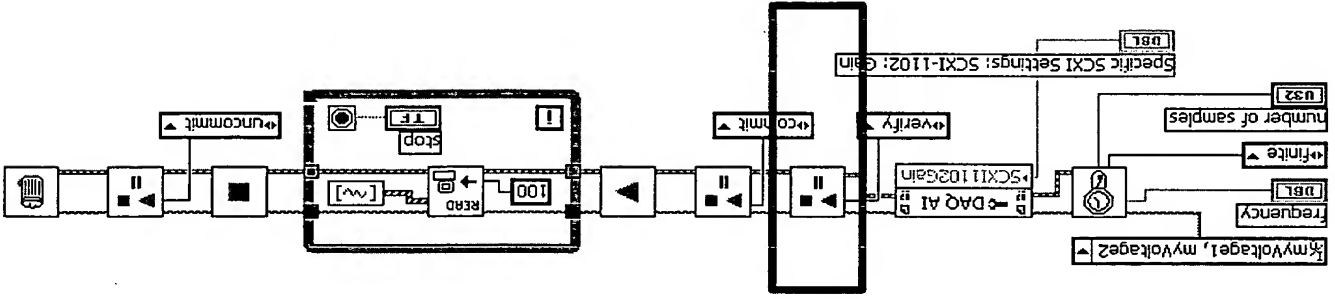
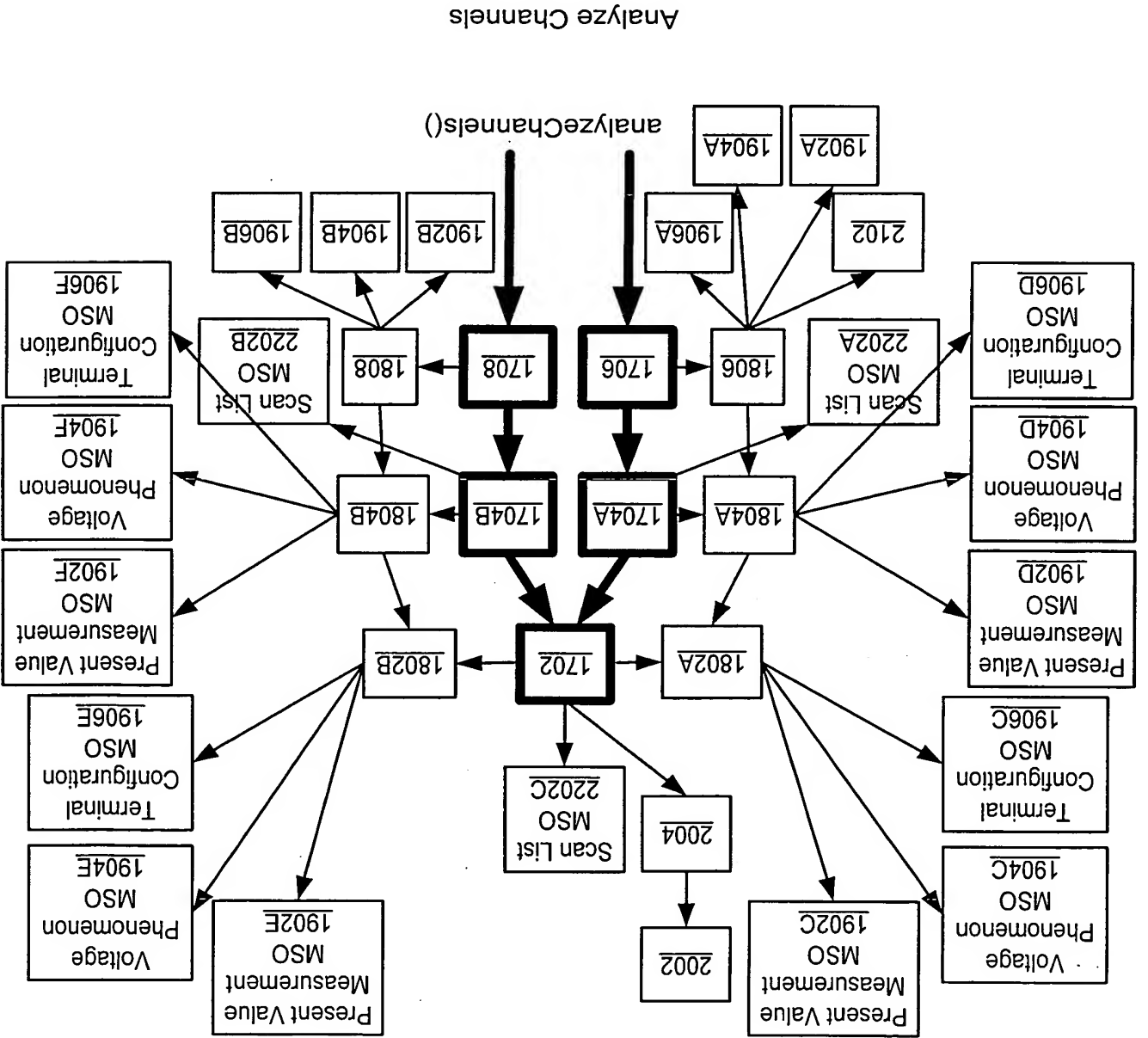


Figure 22





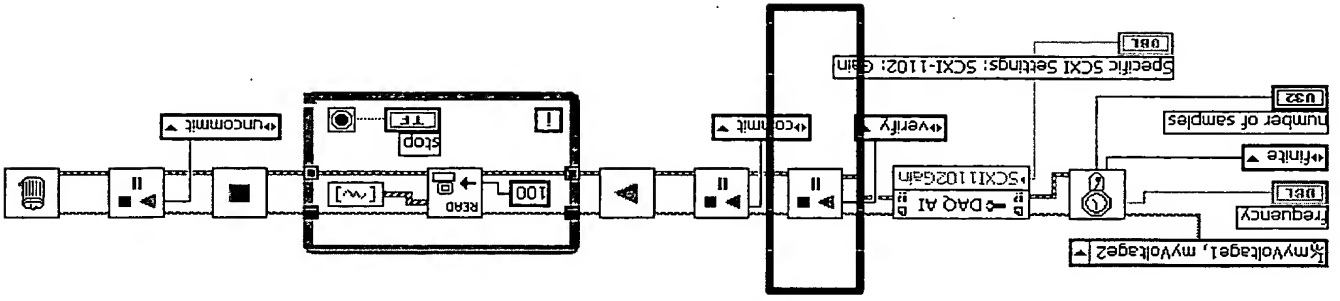
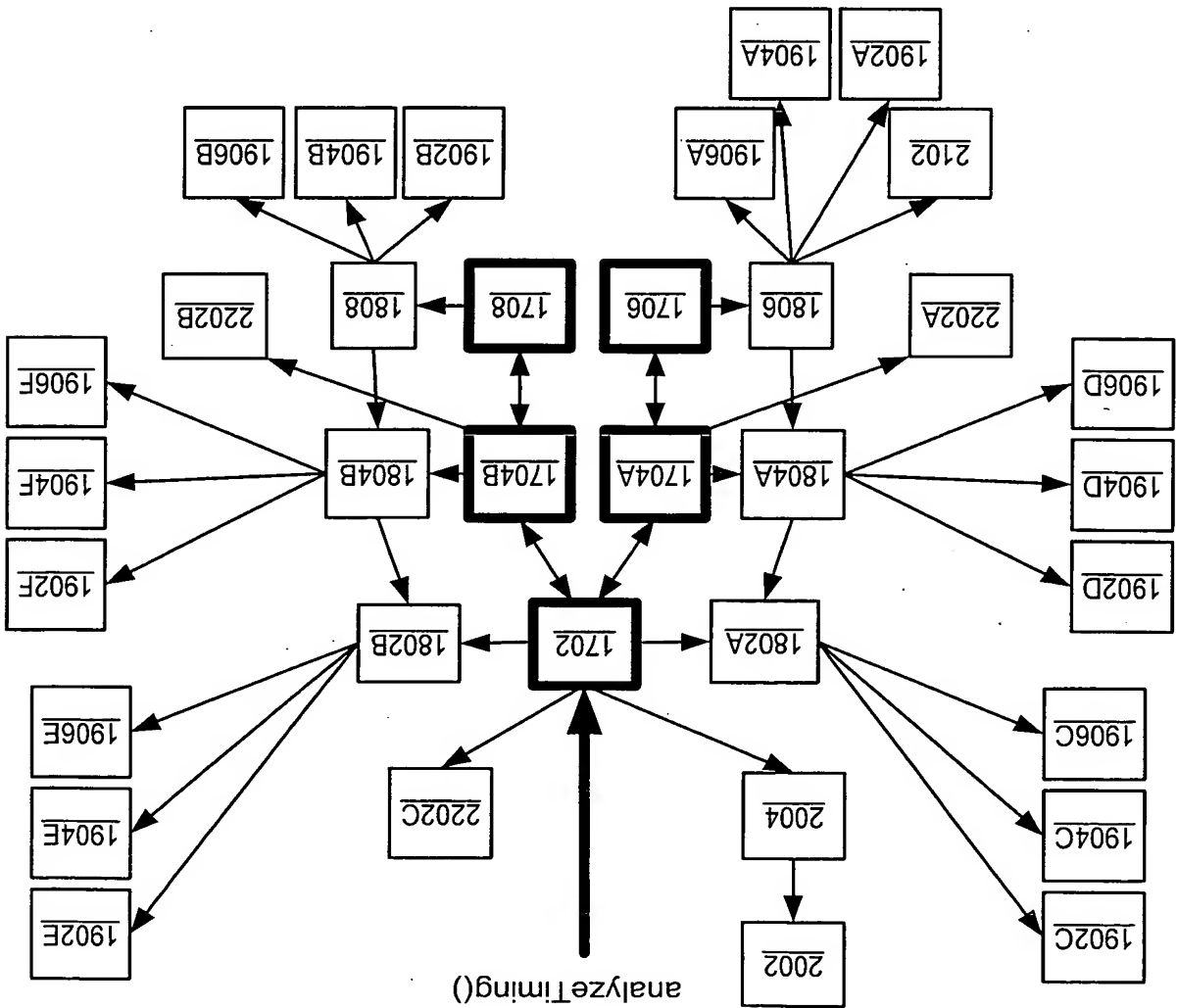


Figure 23

### Analyze Timing



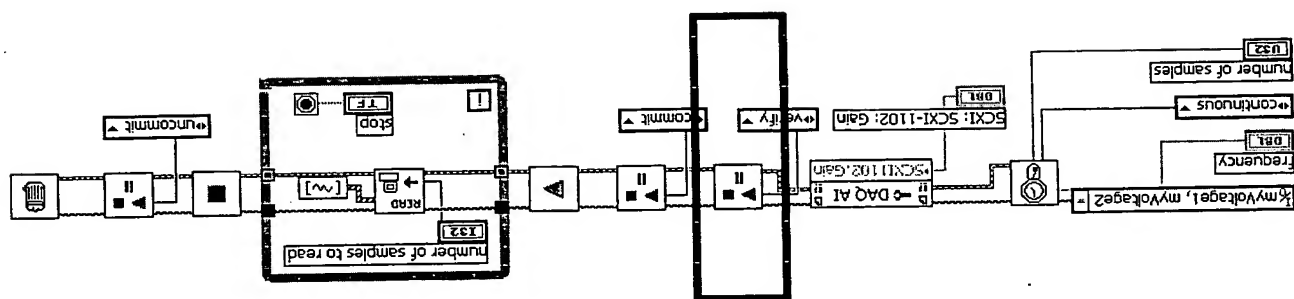
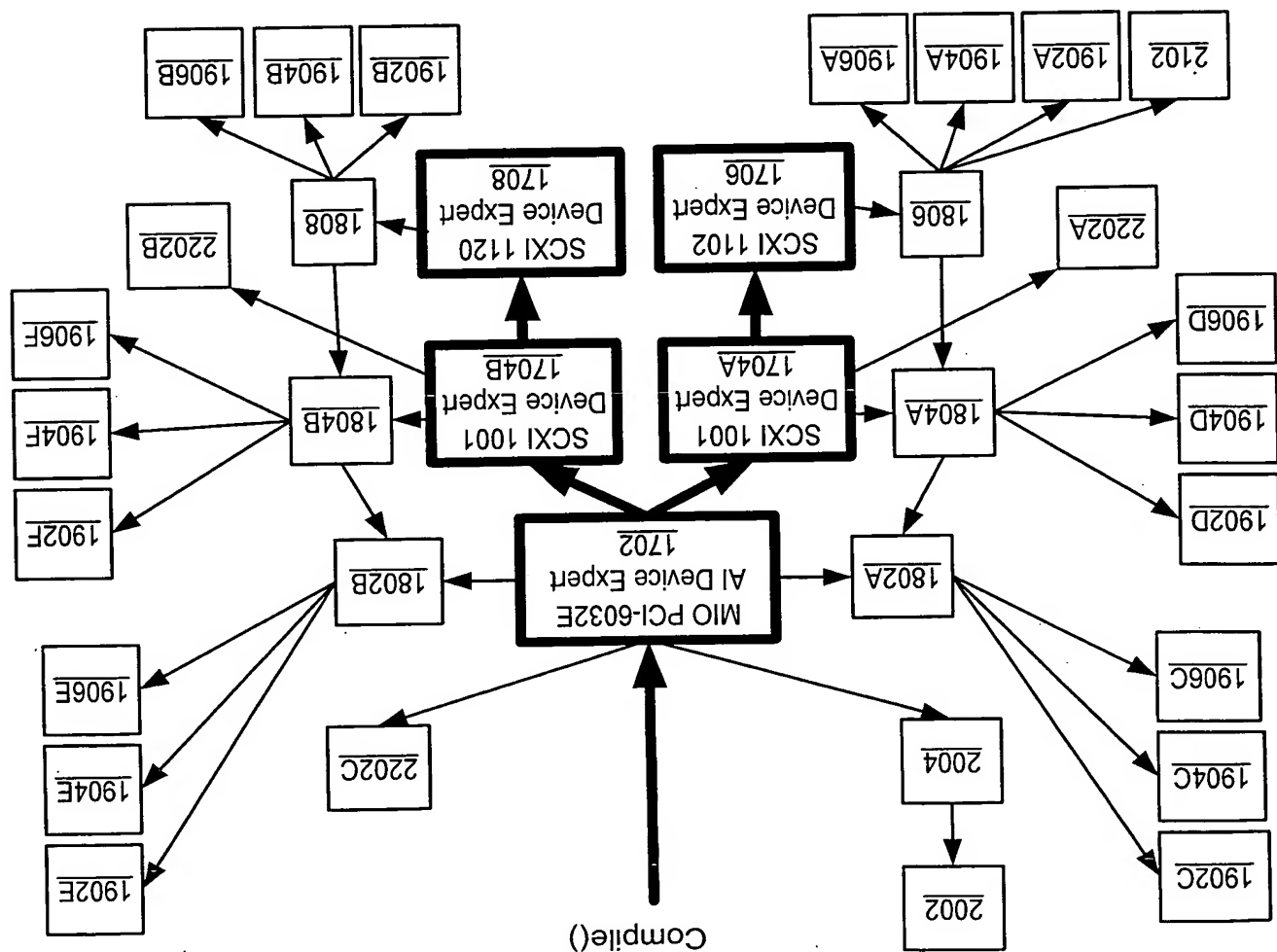


Figure 24A

Compile





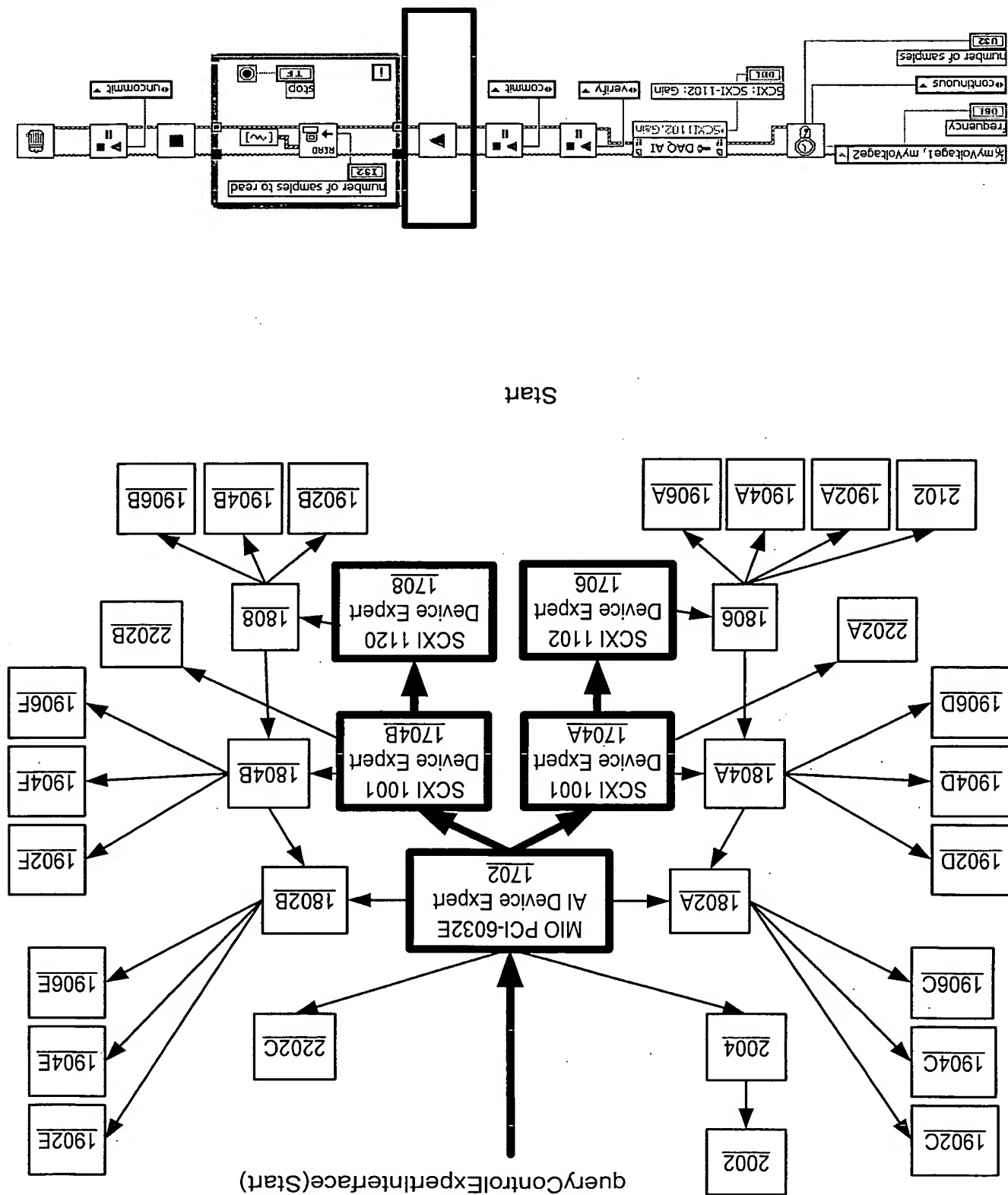


Figure 24C

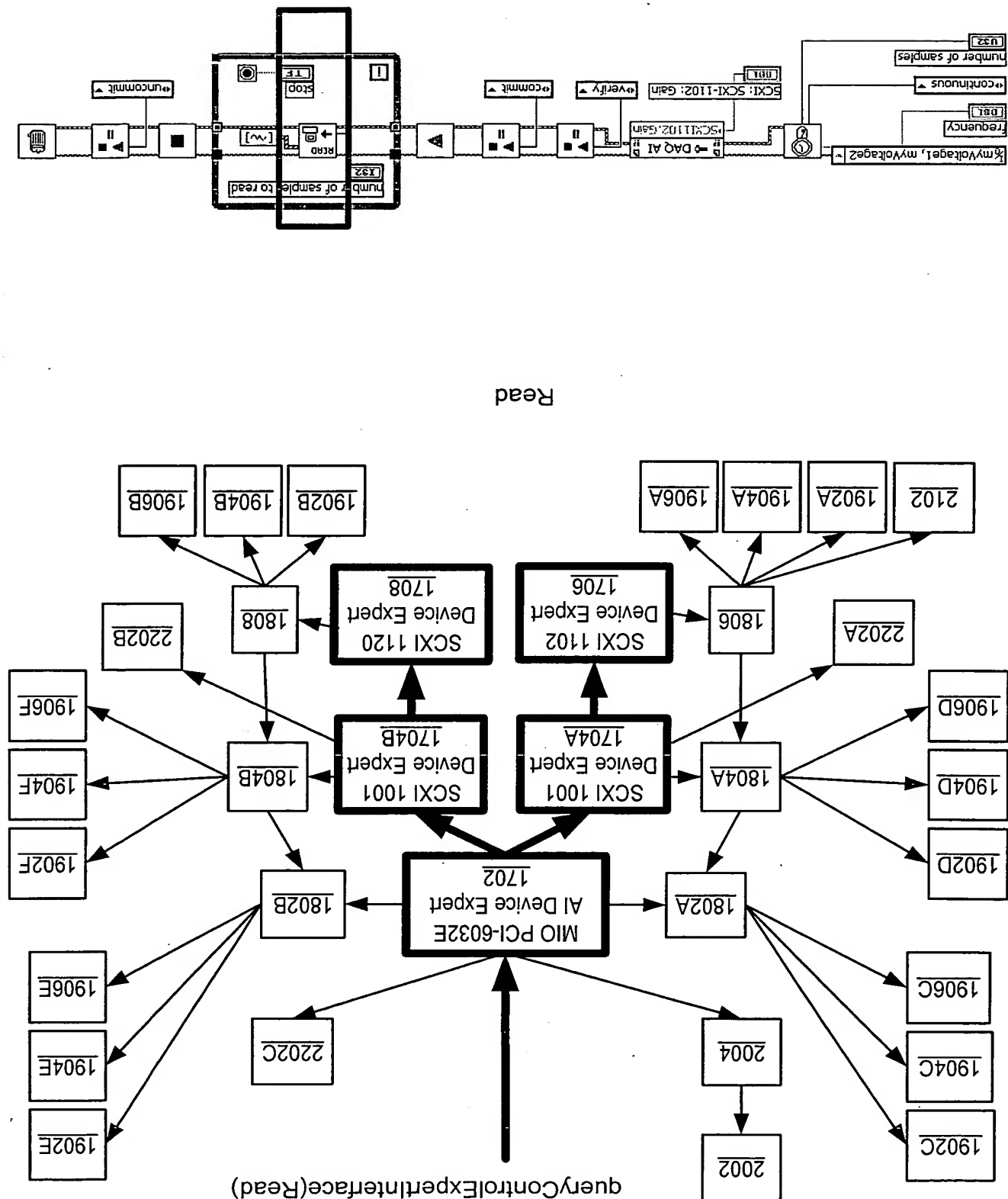


Figure 24D

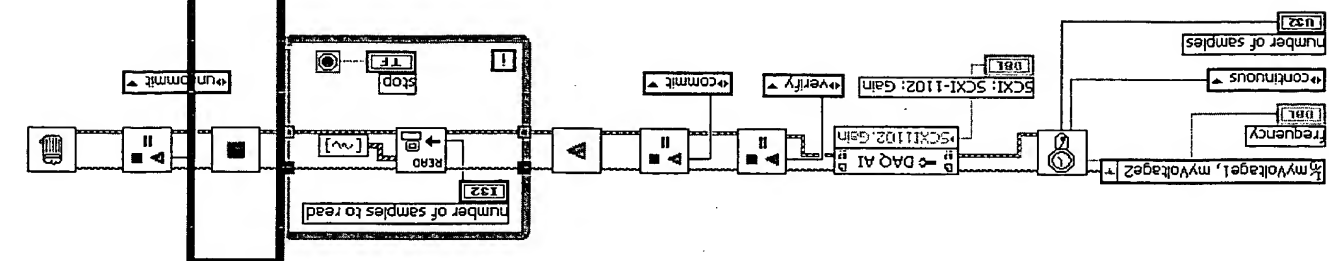
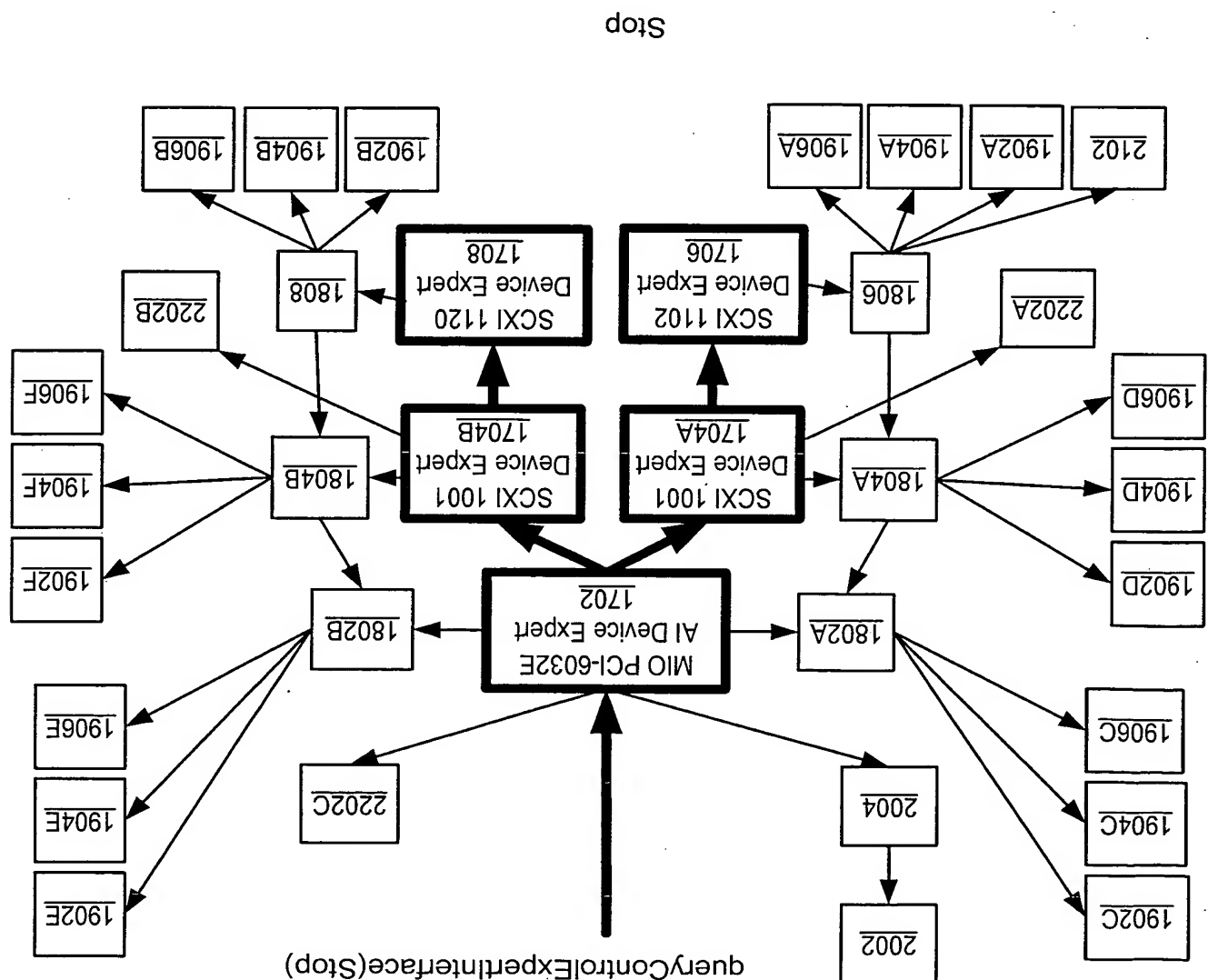


Figure 24E



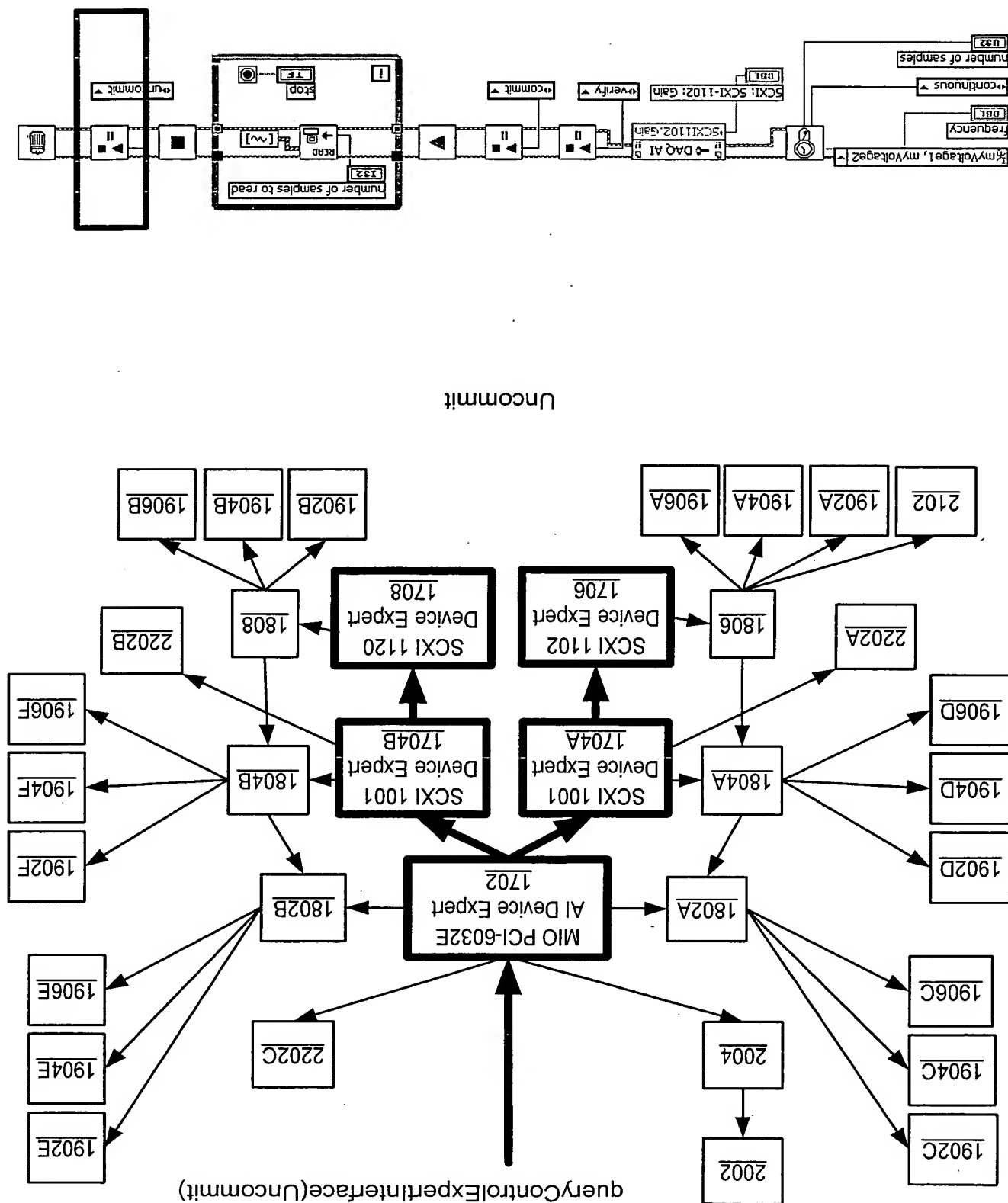


Figure 24F

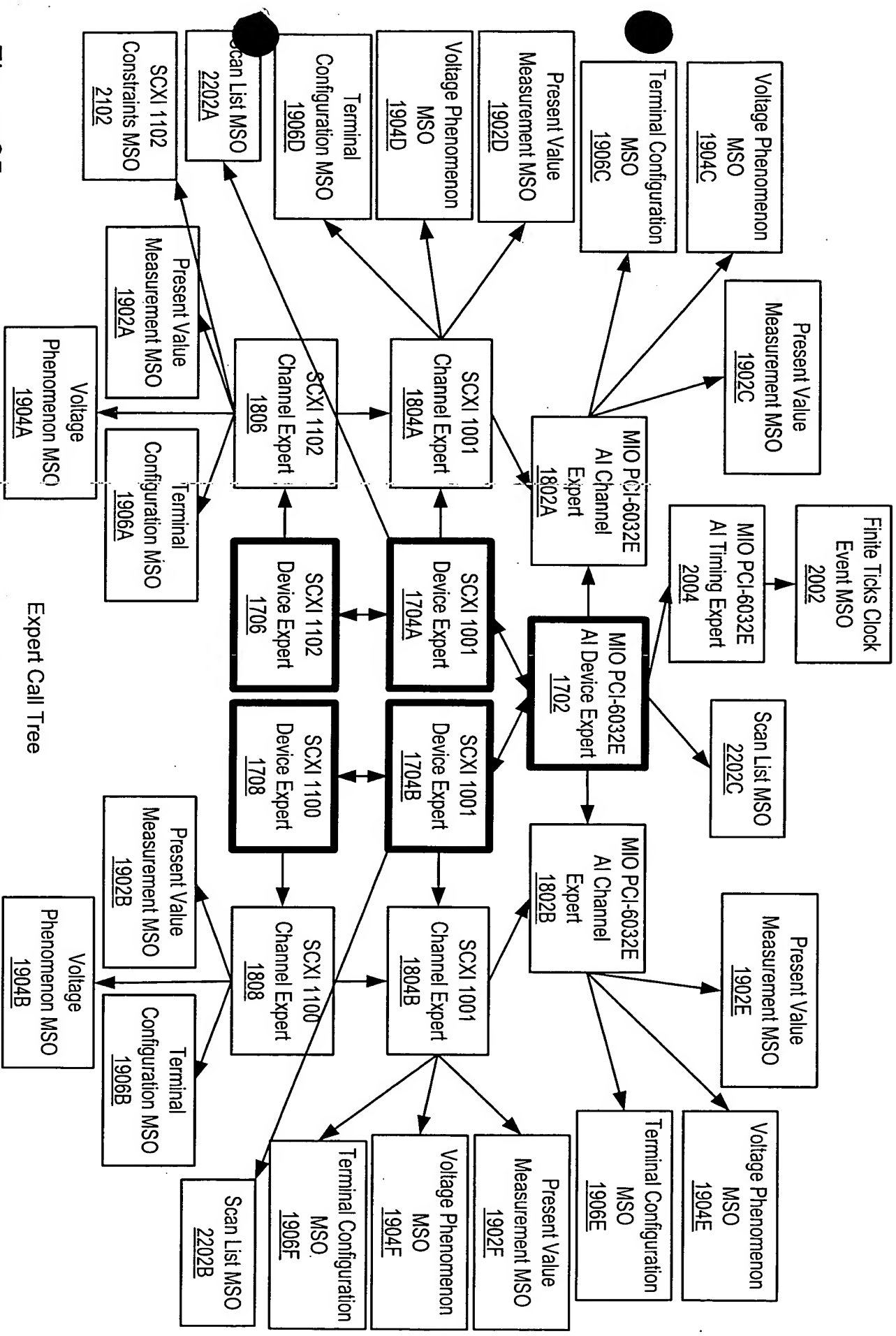


Figure 25

Use Case: Multi-Chassis SCXI Finite Acquisition Using An MIO

Expert Call Tree



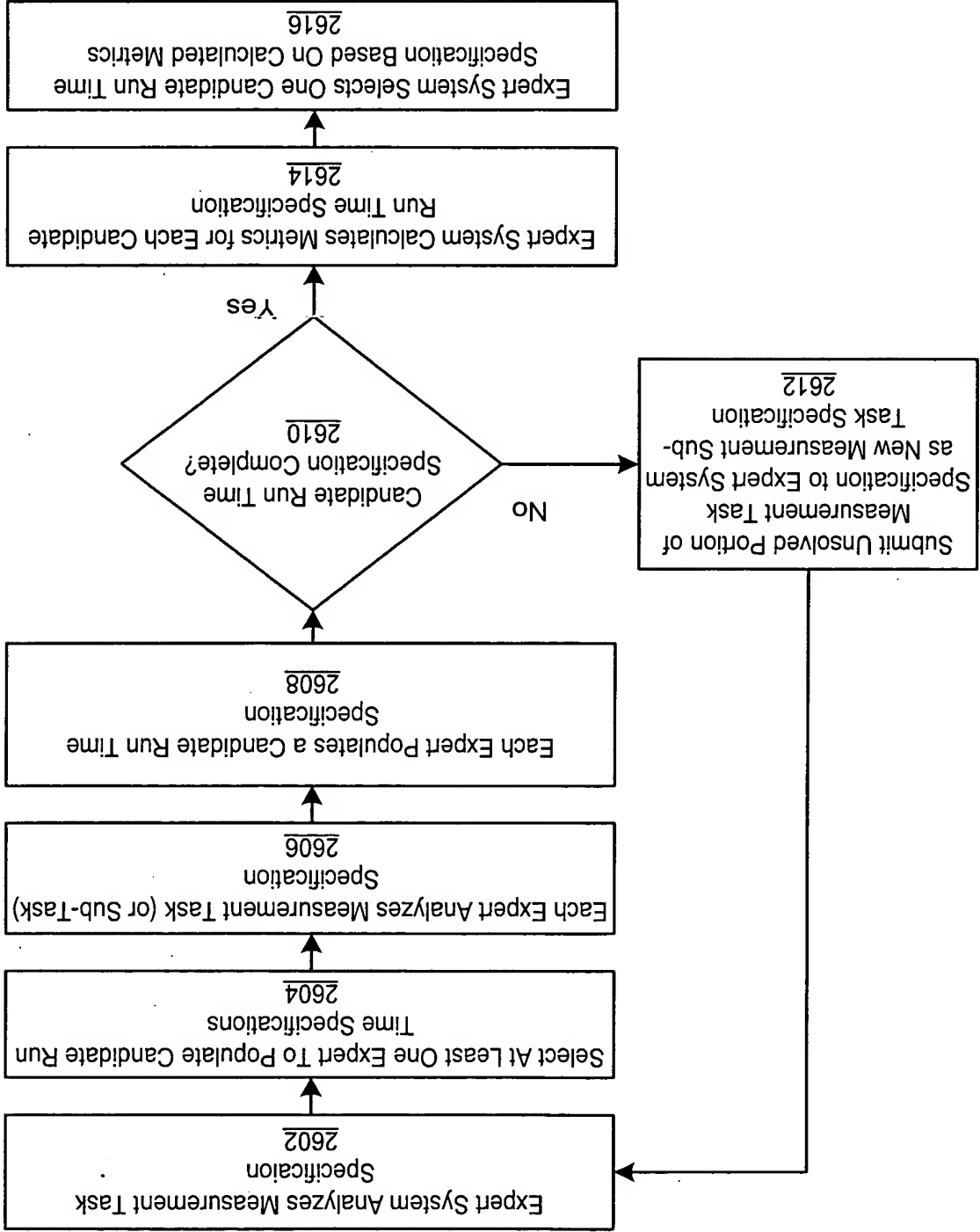


Figure 26

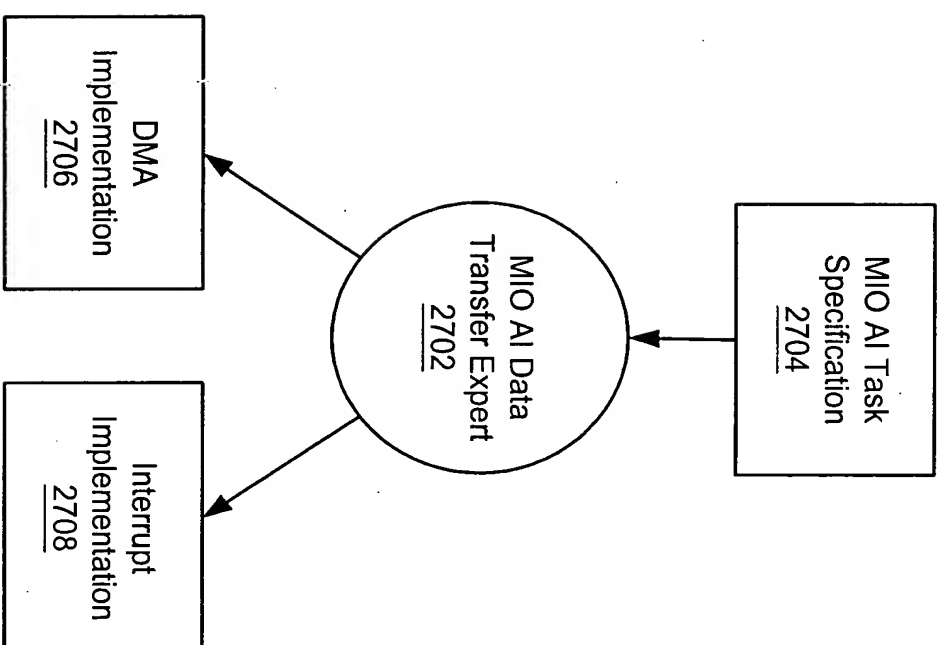


Figure 27

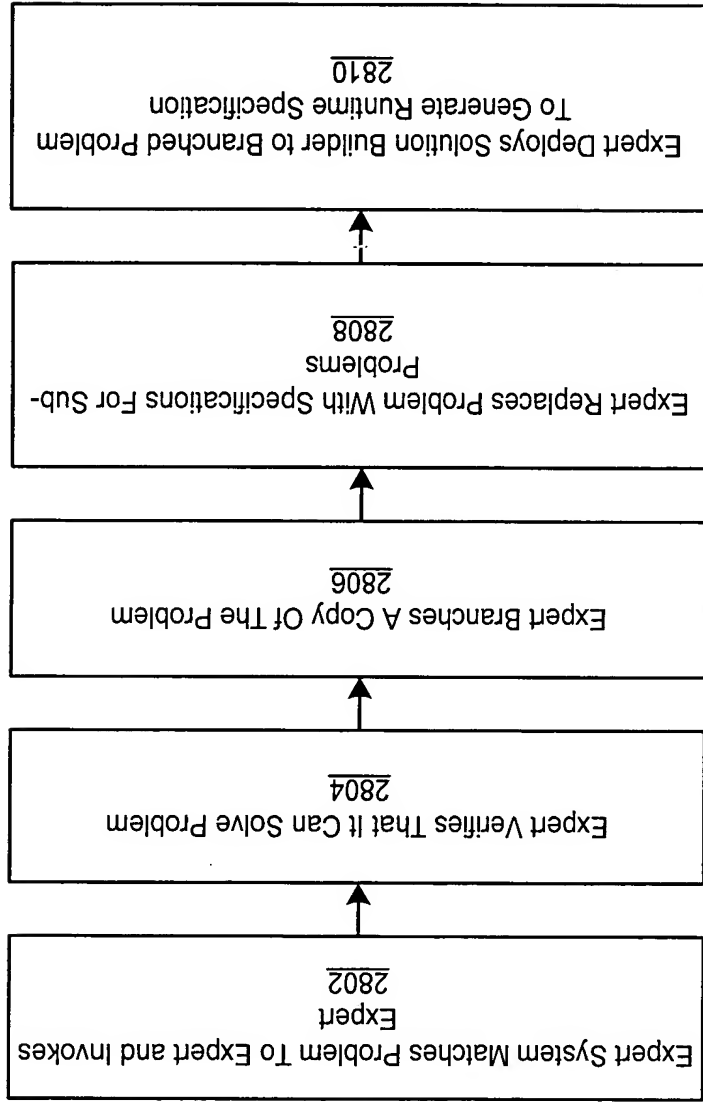


Figure 28

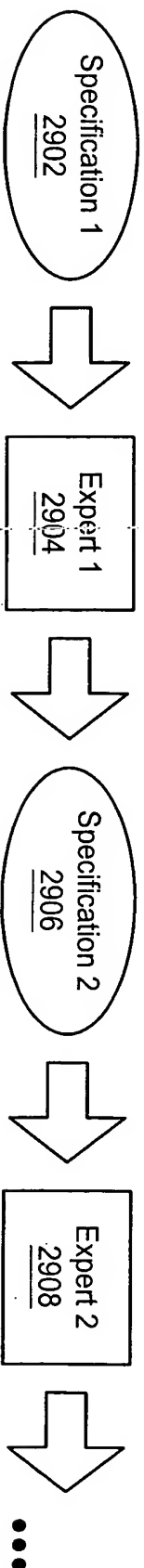


Figure 29

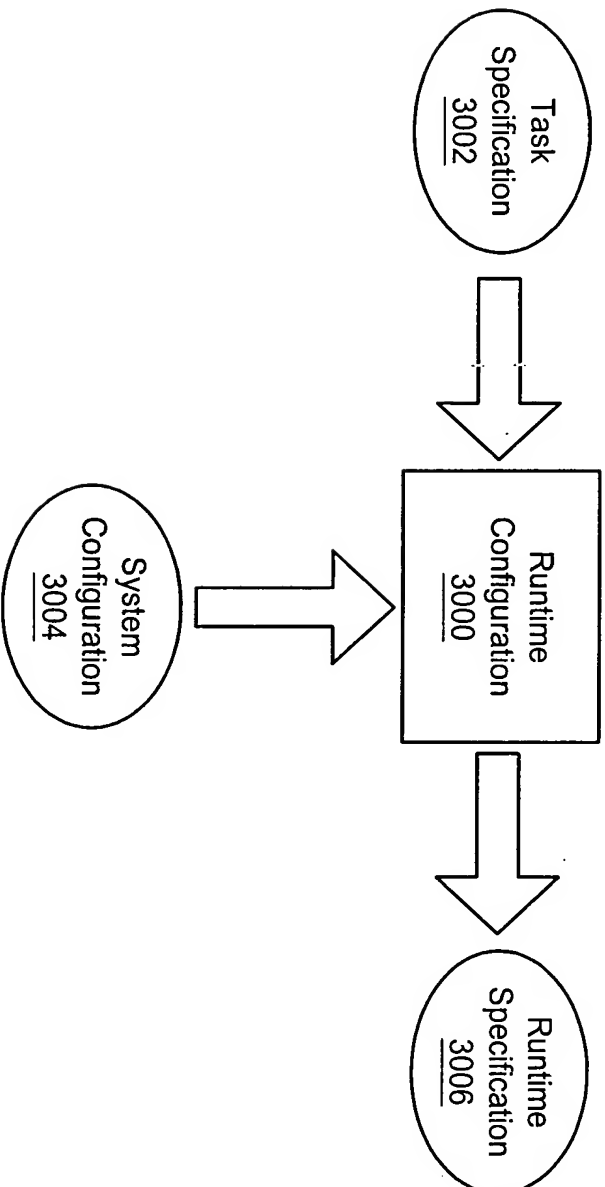


Figure 30

Figure 31

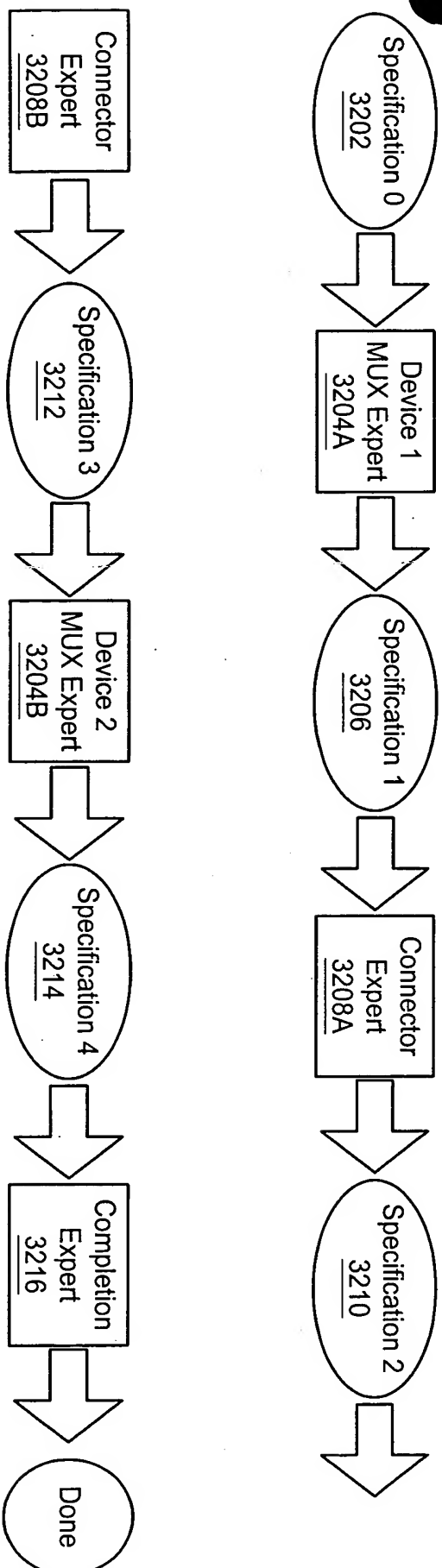


Figure 32

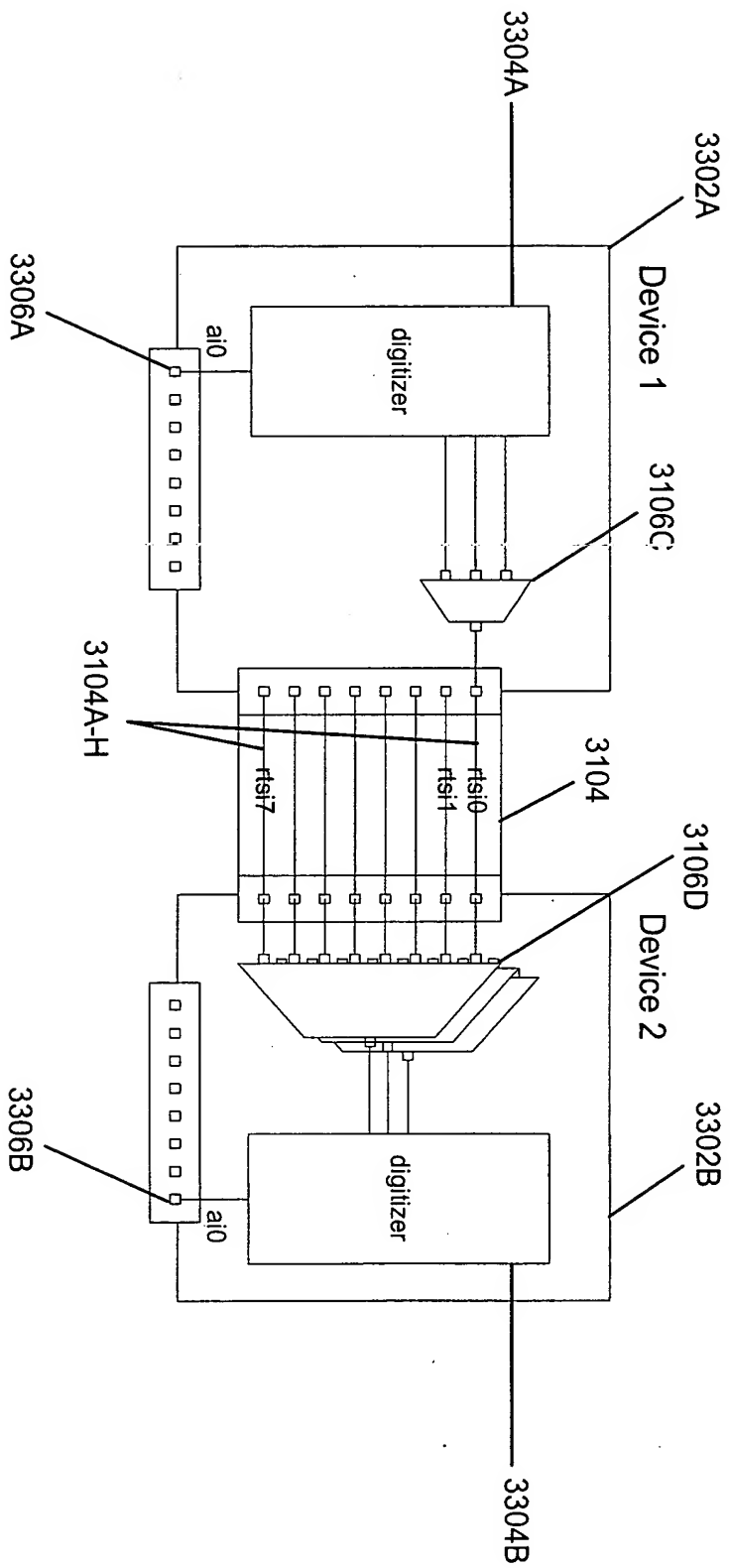


Figure 33



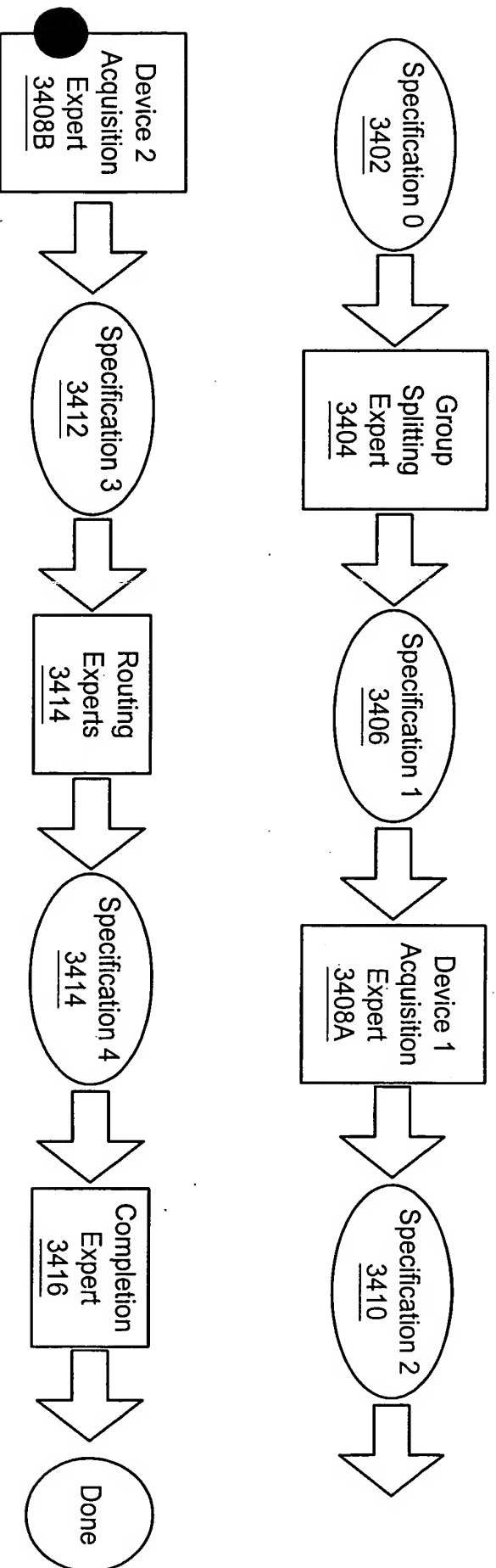


Figure 34

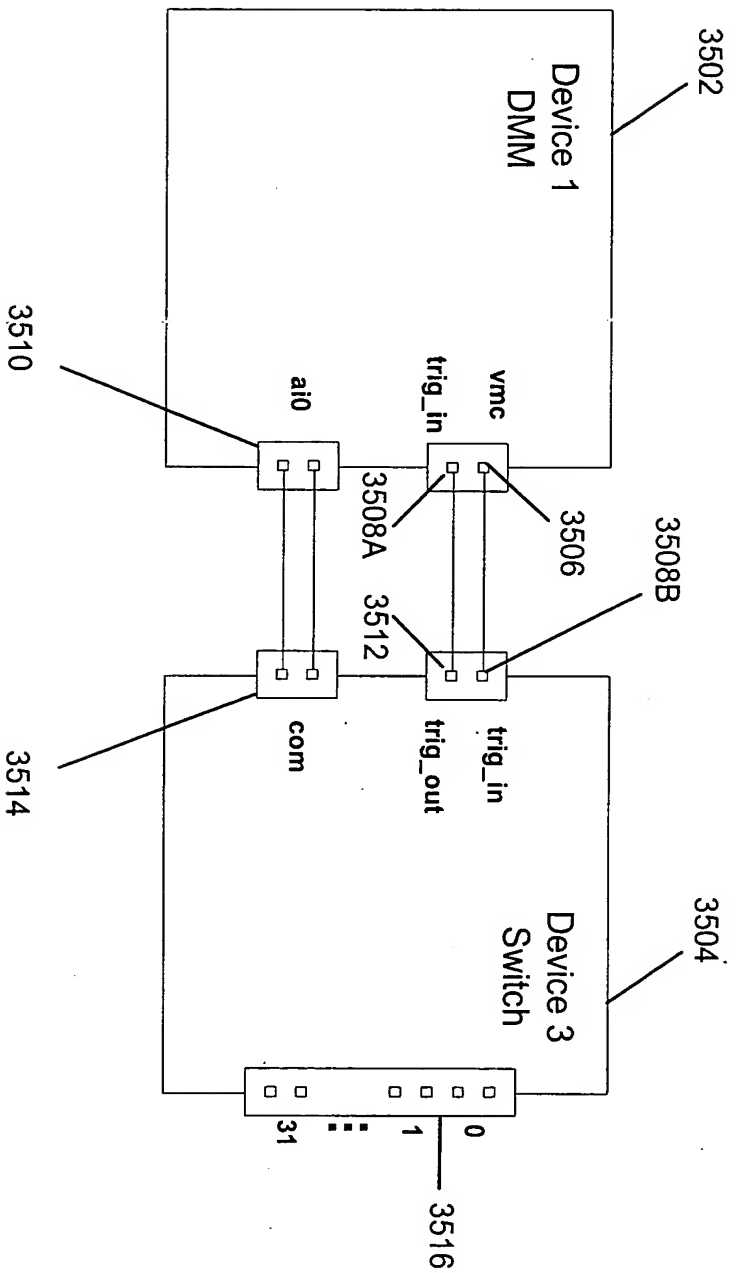


Figure 35

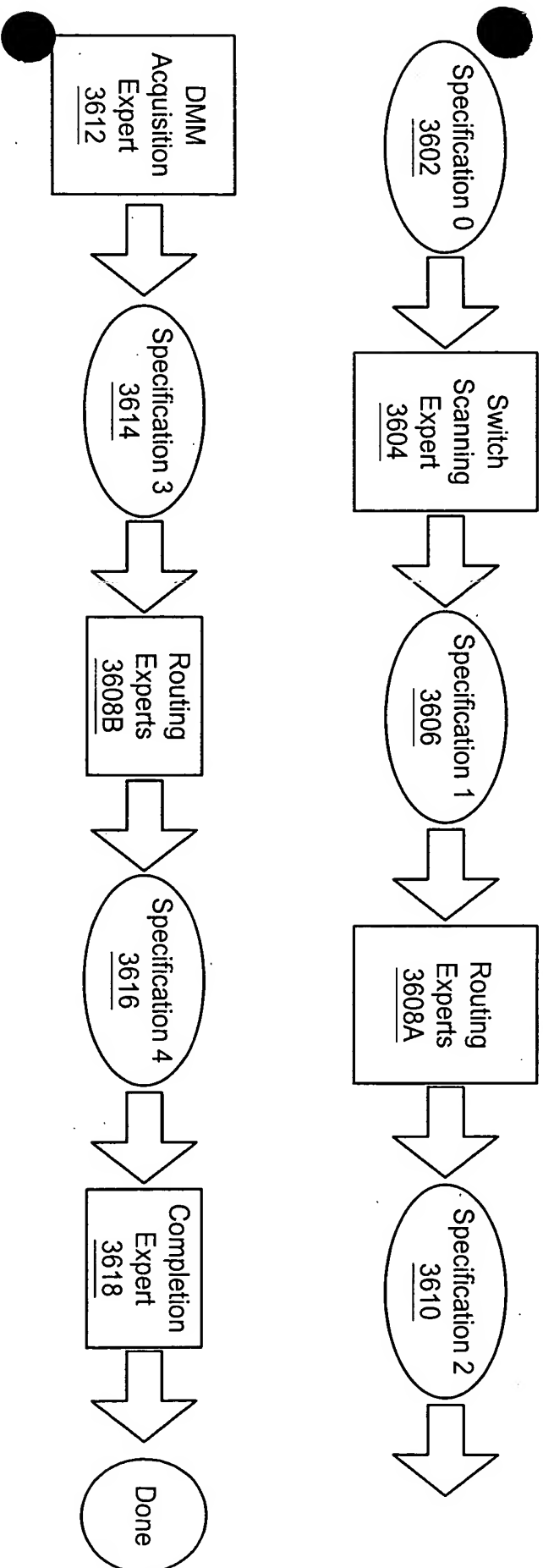


Figure 36

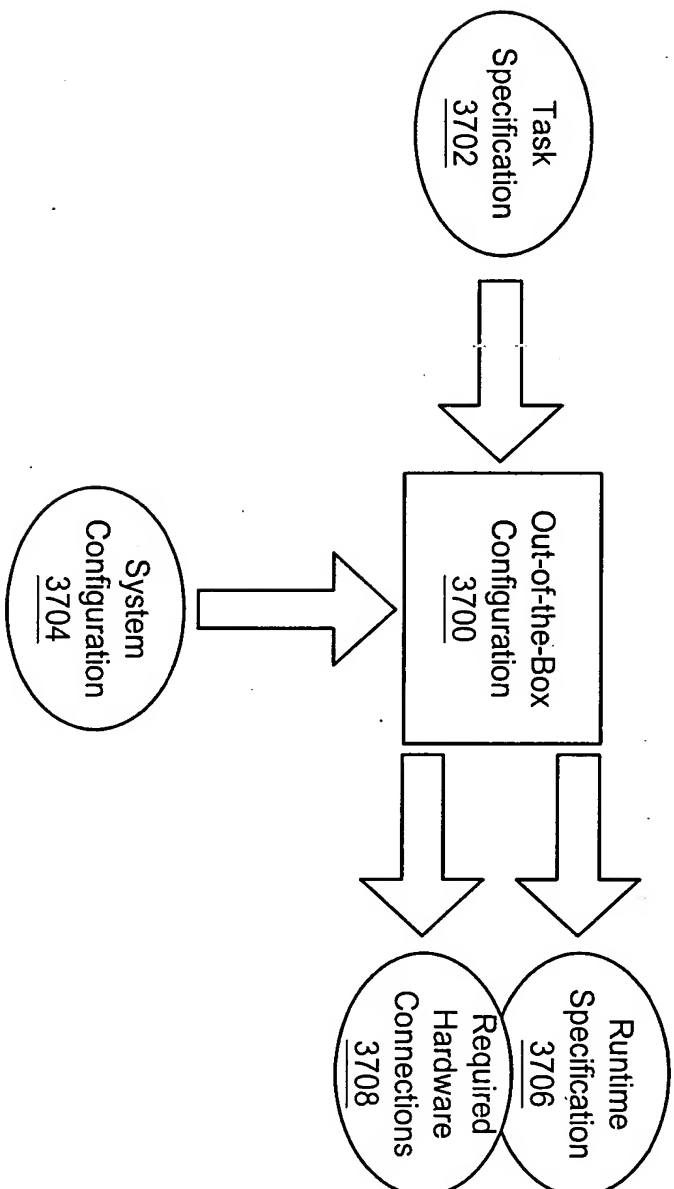


Figure 37

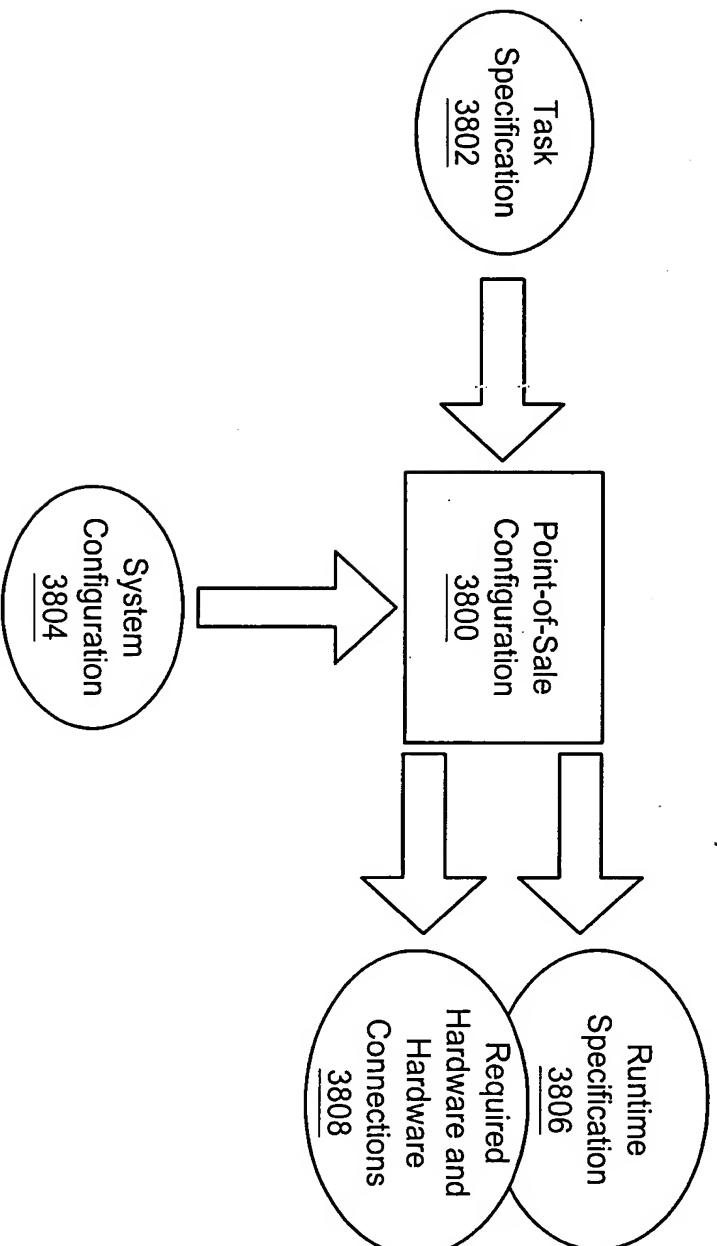
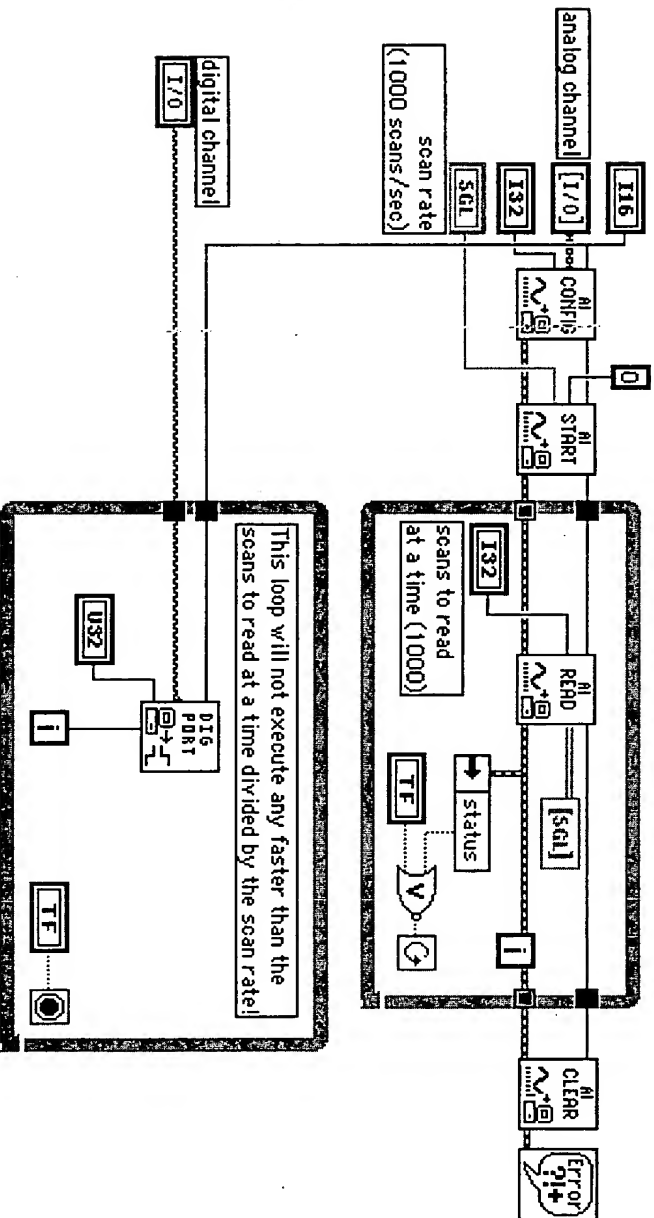
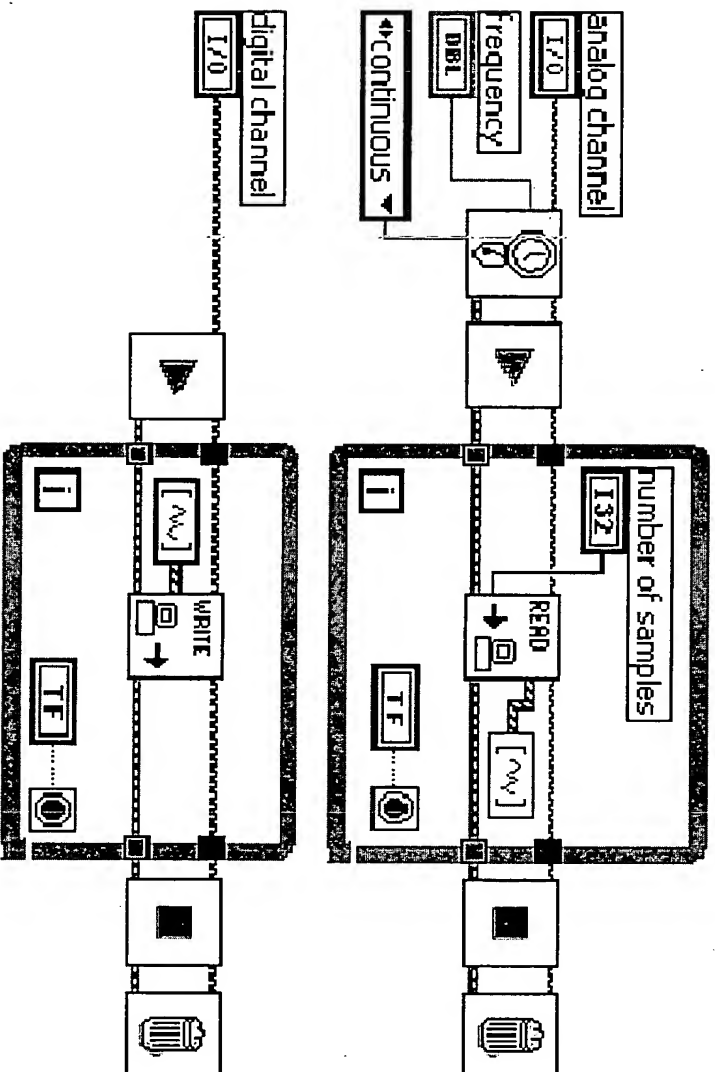


Figure 38



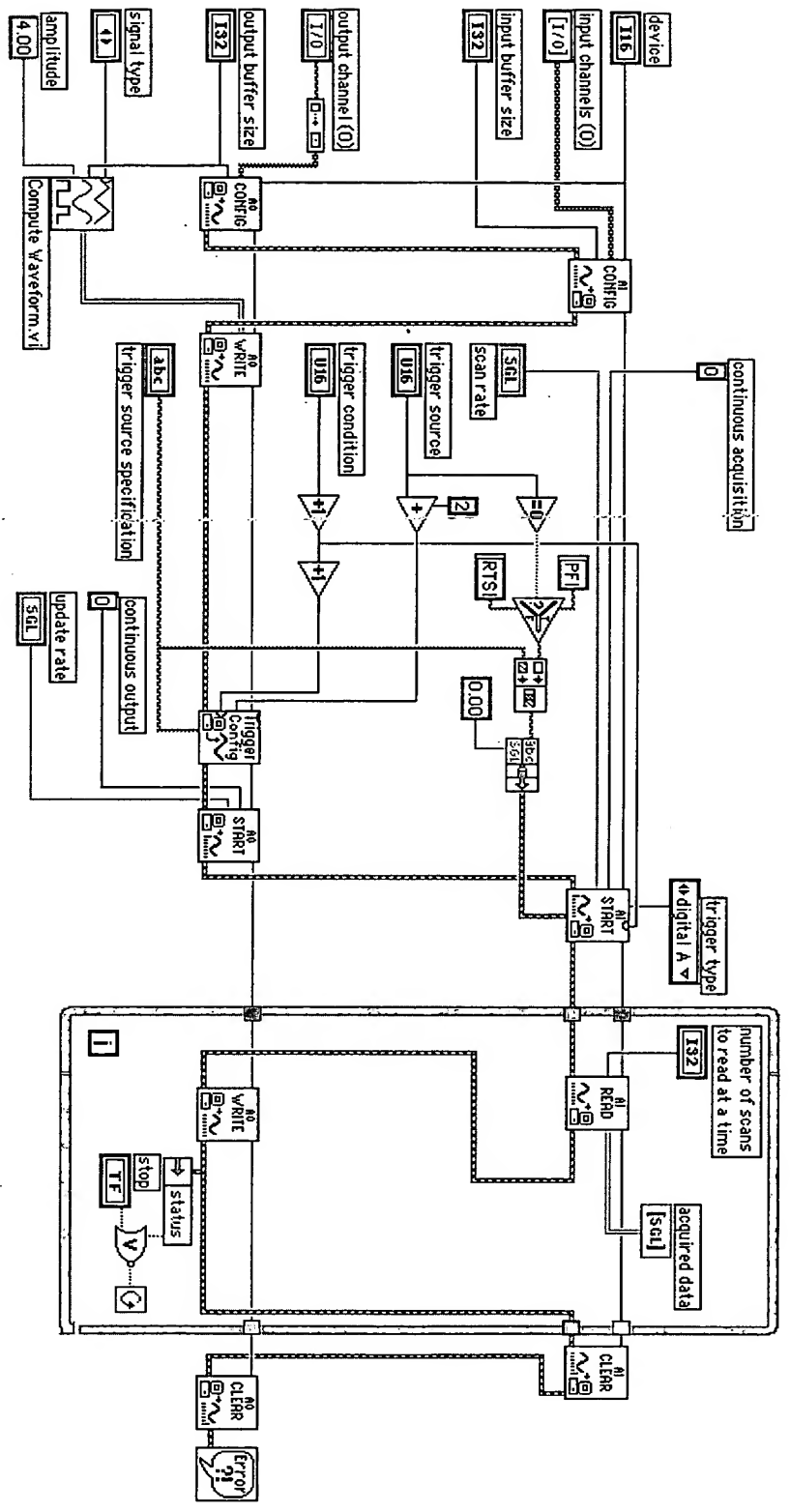
Simultaneous Buffered Analog Input And Single Point Digital  
Output With Single-Threaded Driver (Prior Art)

Figure 39A (Prior Art)



Simultaneous Buffered Analog Input And Single Point Digital Output With Multi-Threaded Driver

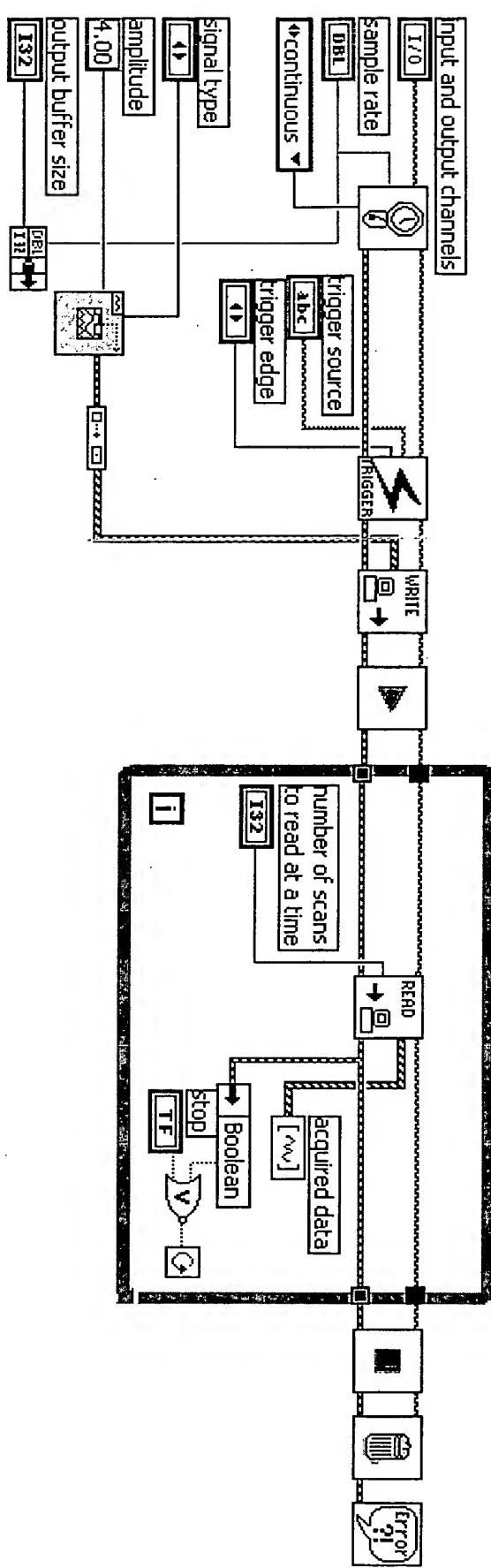
Figure 39B



Simultaneous Triggered Buffered AI/AO (Prior Art)

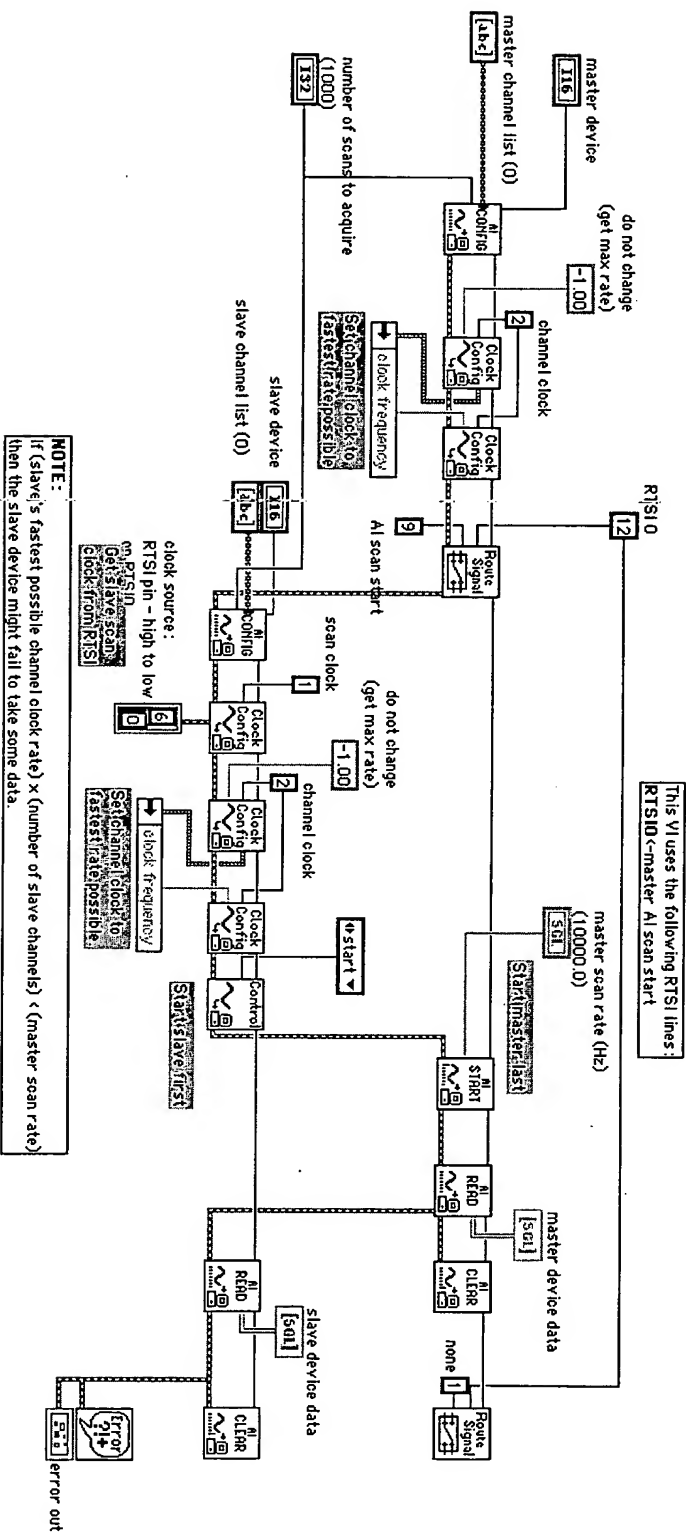
Figure 40A





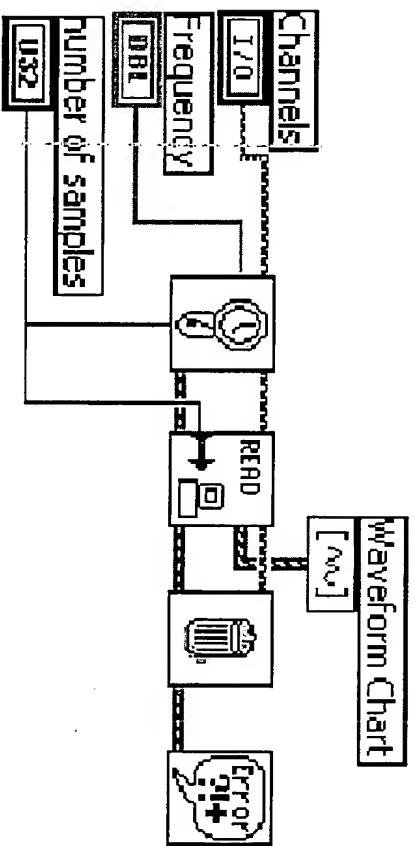
Simultaneous Triggered Buffered AI/AO

Figure 40B



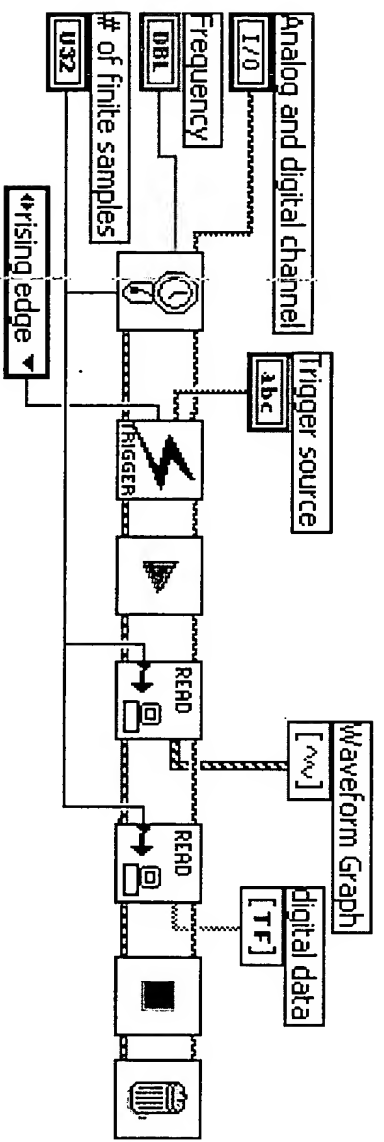
Sharing Scan Clock Across Two E-Series Devices (Prior Art)

Figure 41A



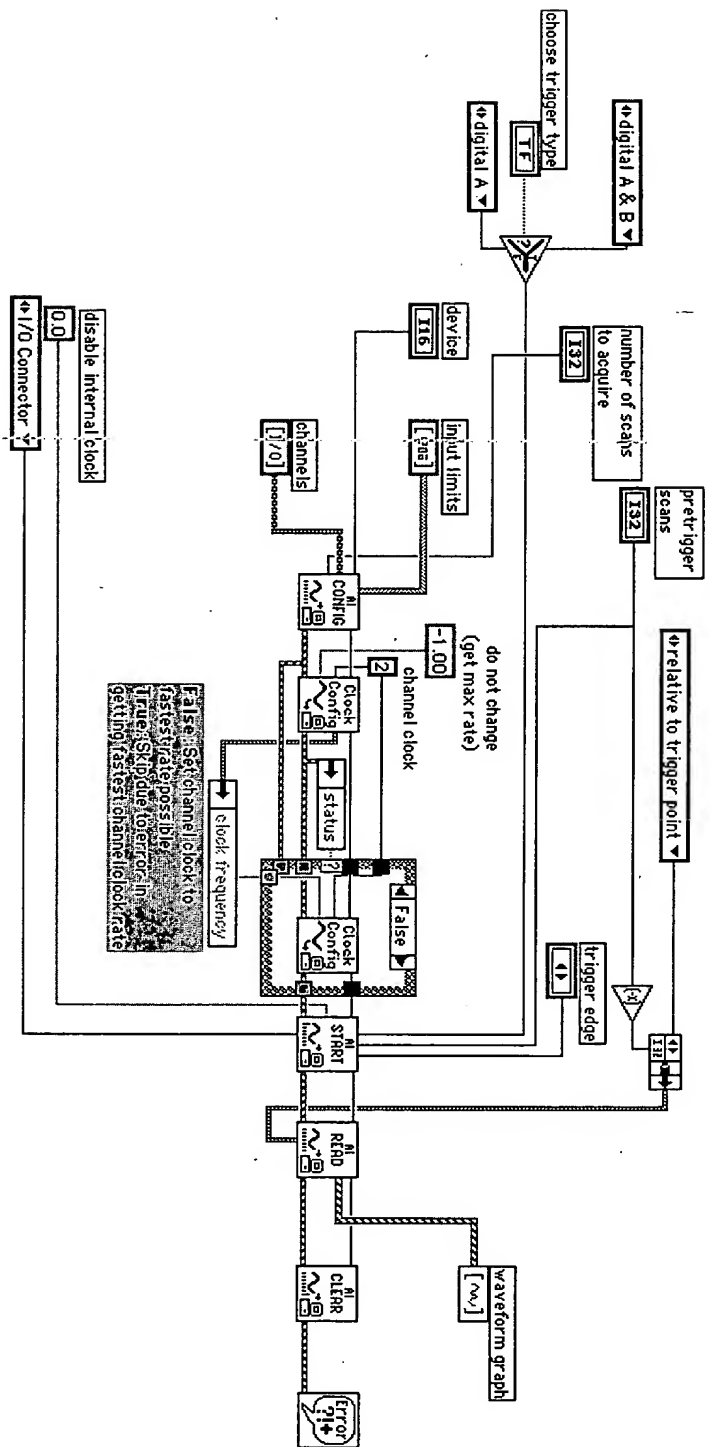
Sharing Scan Clock Across Two E-Series Devices

Figure 41B



Sharing Clock And Trigger, Buffered AI & DI

Figure 42



## Acquire N Scans External Scan Clock Digital Trigger (Prior Art)

Figure 43A (Prior Art)

TOEFT 26280001

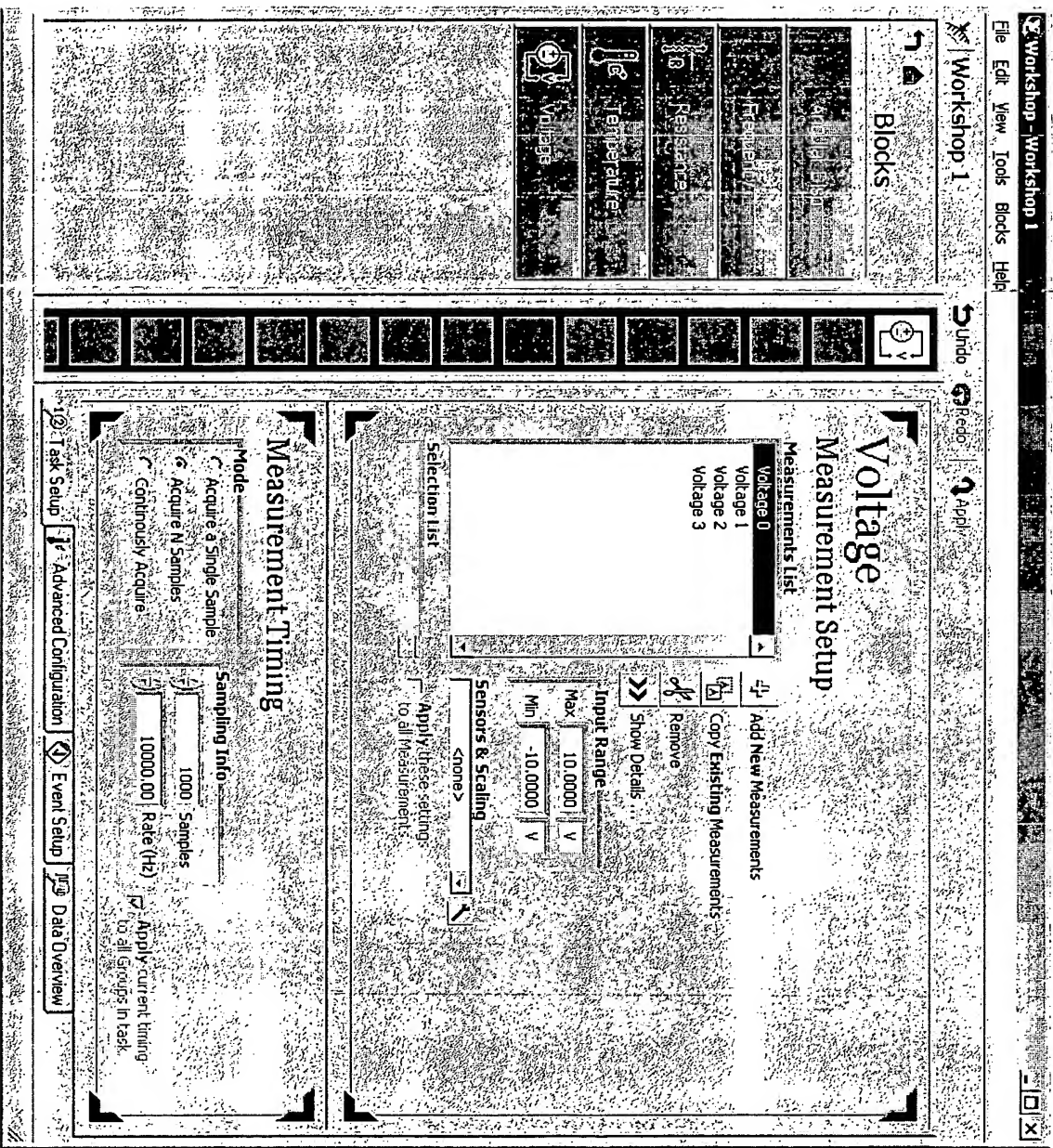


Figure 43B

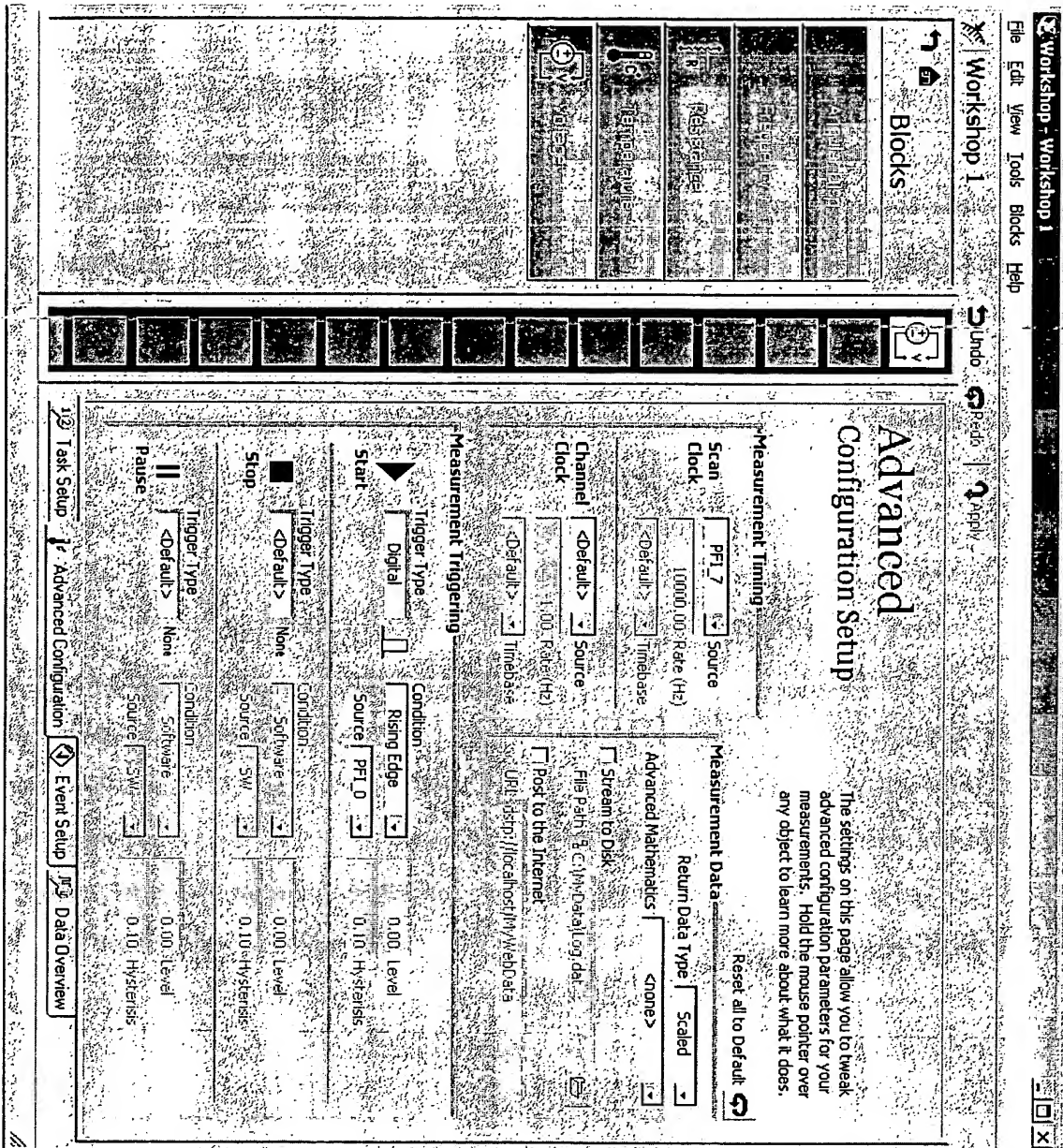
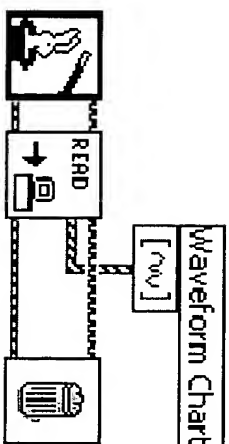


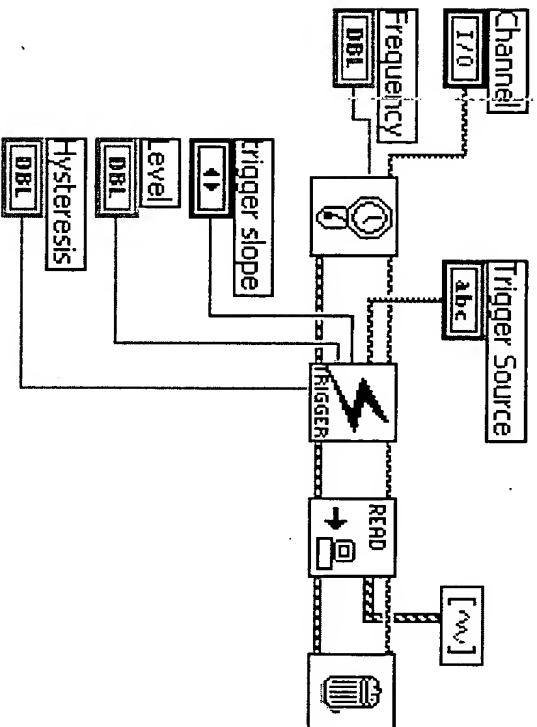
Figure 43C



Acquire N Scans External Scan Clock Digital Trigger

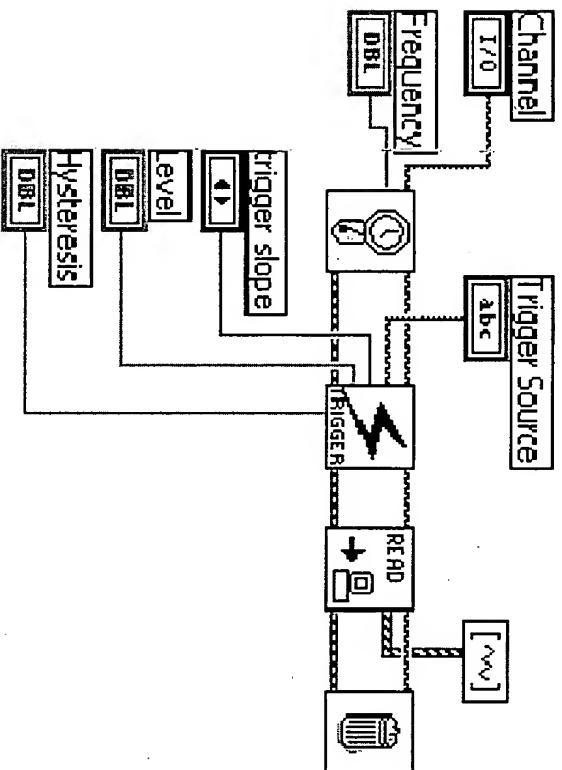
Figure 43D





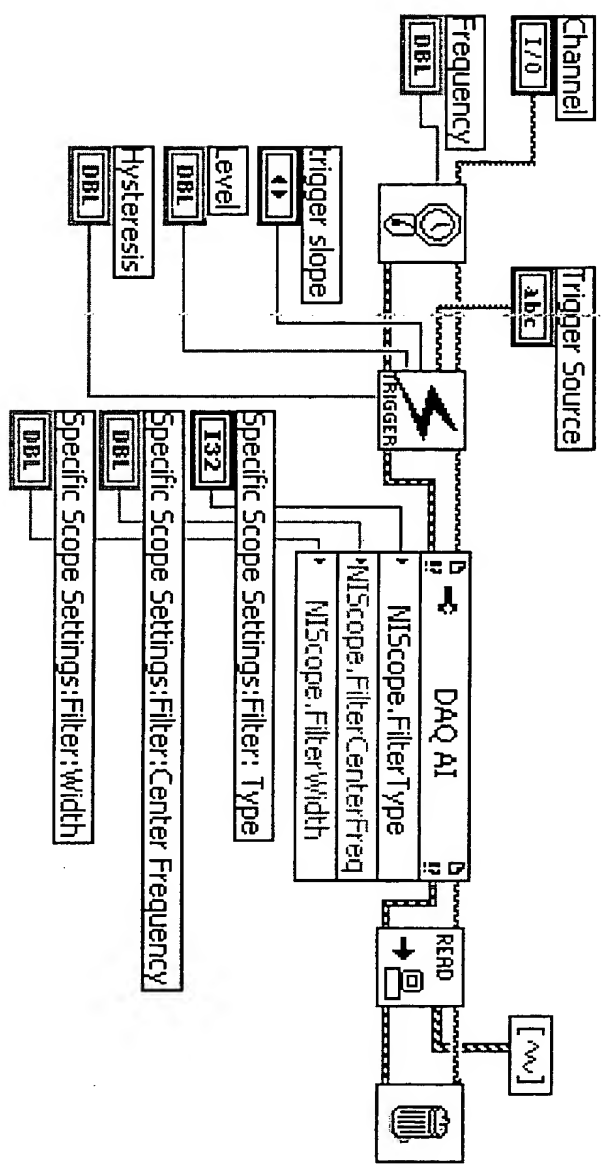
Triggered Acquisition With E-Series Device

Figure 44A



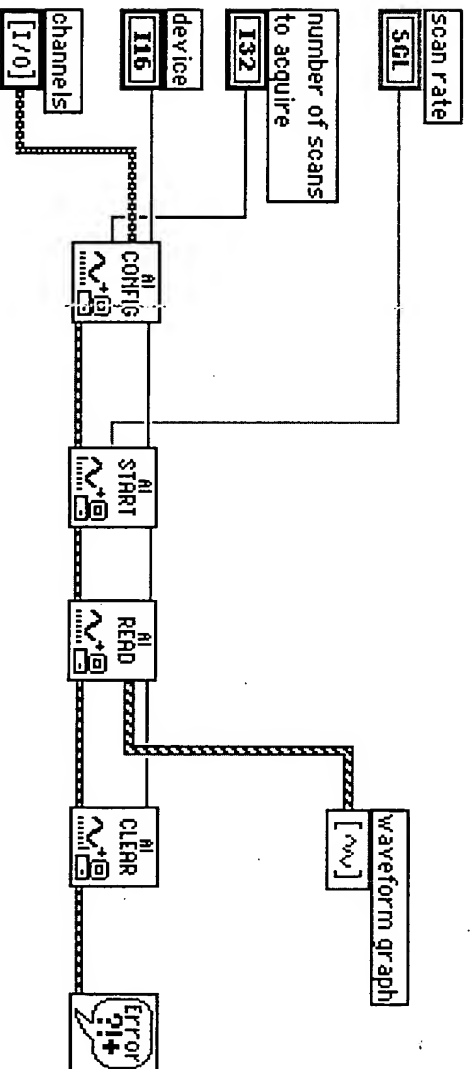
Triggered Acquisition With High Speed Digitizer

Figure 44B



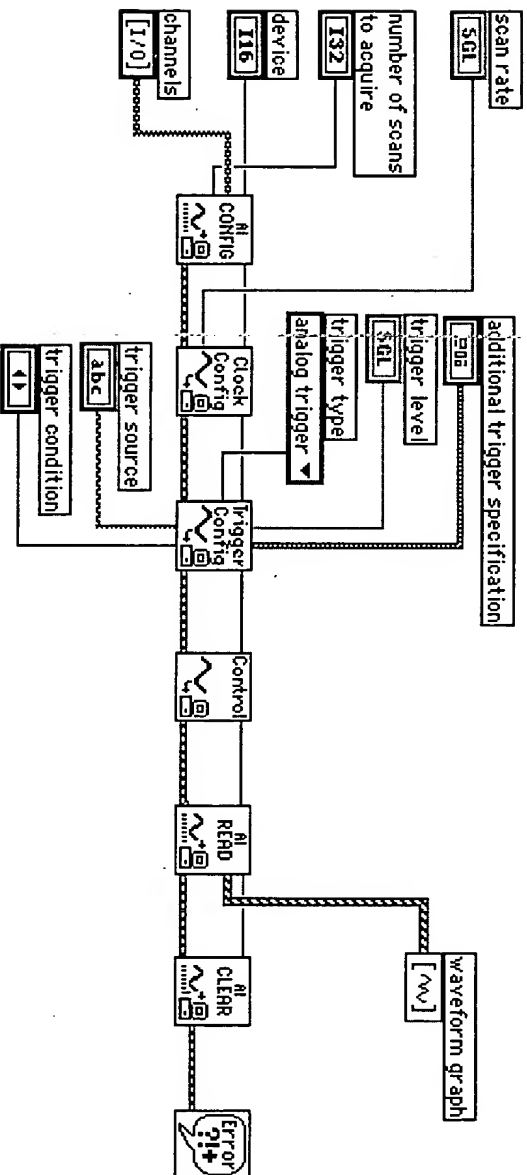
Triggered Acquisition With High Speed Digitizer With Filtering

Figure 44C



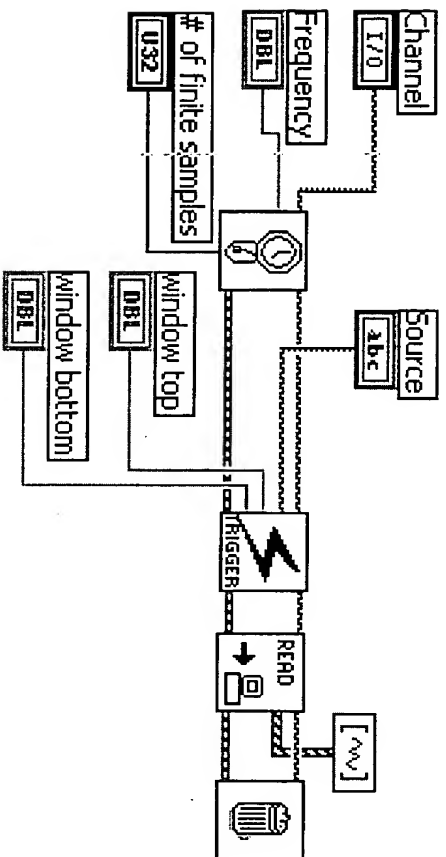
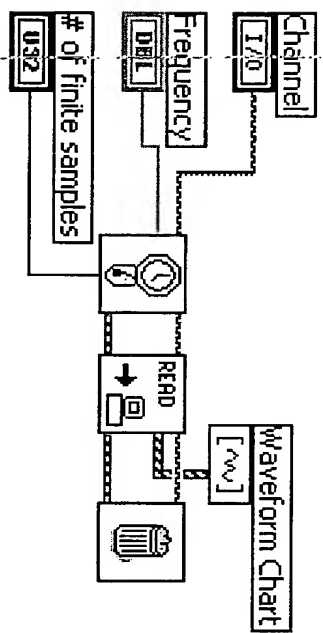
Intermediate Layer (Prior Art)

Figure 45A



Changes For Analog Window Triggering (Prior Art)

Figure 45B



Analog Window Triggering

Figure 45C